STANDARD MICROSYSTEMS
CORPORATION ==========
==========

PUBLICATION 900.006A
JANUARY 8, 1987

A R C N E T

LOCAL AREA NETWORK

CONTROLLER

DESIGNER'S GUIDE

Table of Contents

1.0 GENERAL INFORMATION

1.1 ARCNET-PC FAMILY DESCRIPTION

SMC's ARCNET-PC family of network controller boards provides the user with a simplified interface between the IBM PC bus and an ARCNET modified token passing Local Area Network. The ARCNET-PC, in addition, provides the complete controller for the local area network, which results in virtually user transparent network operation and control.

The ARCNET local area network was originally developed by the Datapoint Corporation as a high performance local area network used to interconnect sophisticated computing systems. Now the performance capabilities of this network are available to users of IBM PC and PC compatible computer systems. The ARCNET-PC family incorporates the Standard Microsystems single chip COM 9026 Local Area Network Controller and COM 9032 ARCNET Local Area Network Transceiver LSI circuits to provide complete ARCNET protocol handling on a single board. A 2K on-board Data Packet Buffer is used to provide four pages of packet storage. This may be dynamically user defined to provide double buffering for both transmit and receive functions. The controller may be polled or interrupt driven. An on-board 8K PROM socket is available to the user for auto boot PROM installation thus enabling a floppy-less PC to access a Local Area Network. The memory mapped Data Packet Buffer, I/O-mapped COM 9026 Controller and 8K PROM socket provide a flexible well rounded PC Local Area Network Controller.

ARCNET-PC100, PC110 - The ARCNET PC100 contains the SMC HYC9068 hybrid RG-62/U coaxial transceiver which connects computers to the ARCNET TOKEN PASSING LOGICAL RING Configuration [i.e. Free Form Tree topology]. The maximum distance for communication between active device units is 2000'. The ARCNET-PC110 contains the same logic, but is a Surface Mounted Half Slot board.

ARCNET-PC200, PC210 - Contains the SMC 9058 High Impedance Transceiver hybrid that allows up to 8 ARCNET- PC200's to be daisy chained over a maximum distance of 1000'.The PC210 is a short slot SMT version of the ARCNET-PC200 and both these units are compatible with the PC100, PC110's.

ARCNET-PC300, PC310 - Contains a Fiber Optic Transceiver hybrid that will allow ARCNET-PC300'S, PC310's to communicate over a distance of 4000' between active units and is well suited as a transmission medium in a high noise/RF environment. The ARCNET-PC310 is a half slot Surface Mount Devices version of the ARCNET-PC300.

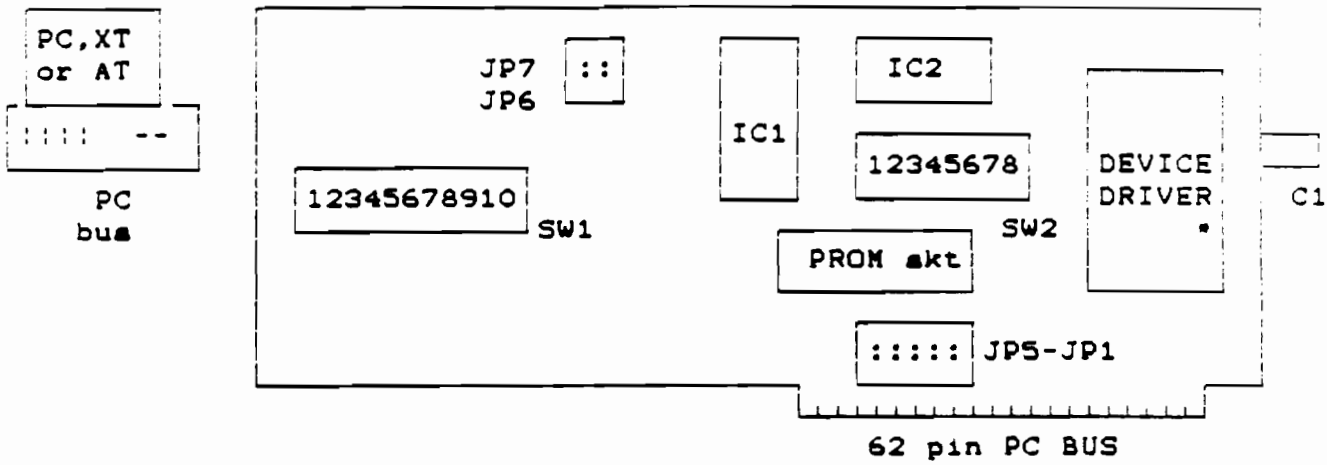
1.2 ARCNET FAMILY FEATURES :

- Provides a simplified interface between IBM/IBM compatible personal computers and the ARCNET modified token passing Local Area Network.
- Compatible with ARCNET baseband coax transmission network
- Uses Standard Microsystems' COM 9026 LAN Controller and COM 9032 LAN Transceiver to simplify the physical and link level ARCNET protocols.
- Supports up to 255 nodes per network segment
- Complete network controller
- 2.5 Megabit data rate
- On-board 2K Data Packet Buffer holds up to four data packets to provide double buffered transmit and receive functions
- Multi transmission media capability
  - COAX CABLE, FIBER OPTIC
- On-board Transceiver hybrid provides greater reliability
- On-board 8K x 8 PROM socket
- Base address of 8K PROM and Data Packet Buffer is switch selectable in 64K segments
- COM 9026 I/O base address is switch selectable in 16 byte segments
- Controller may be polled or interrupt driven with interrupts jumpered to IRQ2, IRQ3, IRQ5, or IRQ7

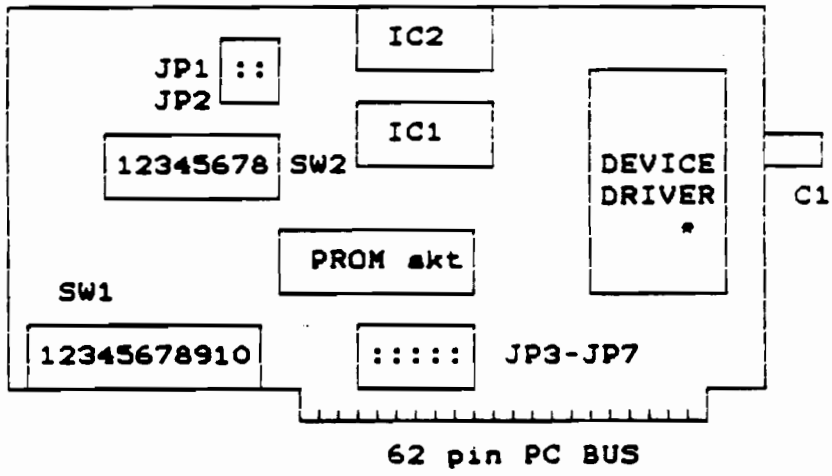
2.0 SPECIFICATIONS

2.1 ARCNET-PC FAMILY BLOCK DIAGRAM

2.1.1 ARCNET- PC100, 200, 300:



2.1.2 ARCNET-PC110, 210, 310:



LEGEND:

C1	BNC RG62 Coax Connector/SMA 200 micron Fiber Optic Connector		
IC1	SMC COM 9026 LAN Controller	SW1 1-6	I/O Address Select
IC2	SMC COM 9032 LAN Transceiver	SW1 7-10	Memory buffer address
		SW2 1-8	Node Address selector

	PC110 TYPE	PC100 TYPE
Extended timeout jumpers:	JP1, JP2	JP3 - JP7
Interrupt selector jumpers:	JP7, JP6	JP5 - JP1

• DEVICE DRIVERS :

ARCNET-PC100, 110 - SMC9068 HYBRID RG62/U COAX TRANSCEIVER
ARCNET-PC200, 210 - SMC9058 HIGH IMPEDANCE RG62/U HYBRID TRANSCEIVER
ARCNET-PC300, 310 - FIBER OPTIC TRANSCEIVER

2.2 PHYSICAL SPECIFICATIONS:

ARCNET Controller:	SMC COM 9026 LAN Controller
Cable Transceiver:	SMC COM 9032 LAN Transceiver
Network Implementation:	Compatible with Datapoint ARCNET LAN network specifications. Uses a base band system with RG62/U (93 ohm) coax or 200 micron step index fiber optic cable.
System Bus:	Compatible with IBM Personal Computer Bus
Memory:	2K x 8 Static Ram Data Packet Buffer 8K x 8 PROM Location
Power Requirement:	+5 volts @ 900 ma. max.* -5 volts @ 42.5 ma. max.
Physical Dimensions	
ARCNET-PC100,200,300:	8.5" by 3.9"
ARCNET-PC110,210,310:	5.25" by 3.9"
Environmental Operation:	0° to 70° C
Coax Connector:	Isolated Ground BNC
Fiber Optic Connector:	SMA 200 micron step index single fiber

* POWER REQUIREMENTS for the PC200,210 would have an increase of 60 ma @ +5 volts
10 ma @ -5 volts

2.3 TOPOLOGICAL SPECIFICATIONS

2.3.1 ARCNET-PC 100,110

The PC100,110 products are used in a Free-Form Tree topology with the following distance restrictions:

1 2000 feet maximum distance between active hubs and/or ARCNET-PC 100,110 controller boards.

2 100 feet maximum distance between passive hub port and an active hub port or ARCNET-PC 100,110 board.

2.3.2 ARCNET-PC 200, 210

The ARCNET-PC 200,210 controller boards are used in a physical Bus Format topology while retaining a logical Token Passing ring format. The topological restrictions are as follows:

1 Maximum bus length of 1000 feet with up to 8 ARCNET-PC200,210 boards tapped off the bus using "T" coaxial connectors.

2 Each end of the bus is to be terminated by either an active hub port or a 93 Ohm terminator.

2.3.2 ARCNET-PC 200, 210 cont.

3 For extended Bus lengths, a single PC200 node on a 1000 foot bus can be replaced by one port of a 2 Port SMC ACTIVE LINK which can then extend the bus an additional 1000 feet with up to 7 ARCNET-PC200, 210 units tapped off.

4 An ARCNET-PC 200 or PC210 CAN be used in place of ARCNET-PC 100 or PC110 if it is used in conjunction with a "T" and Terminator on the PC100 coaxial cable - See diagram.

2.3.3 ARCNET-PC 300, 310

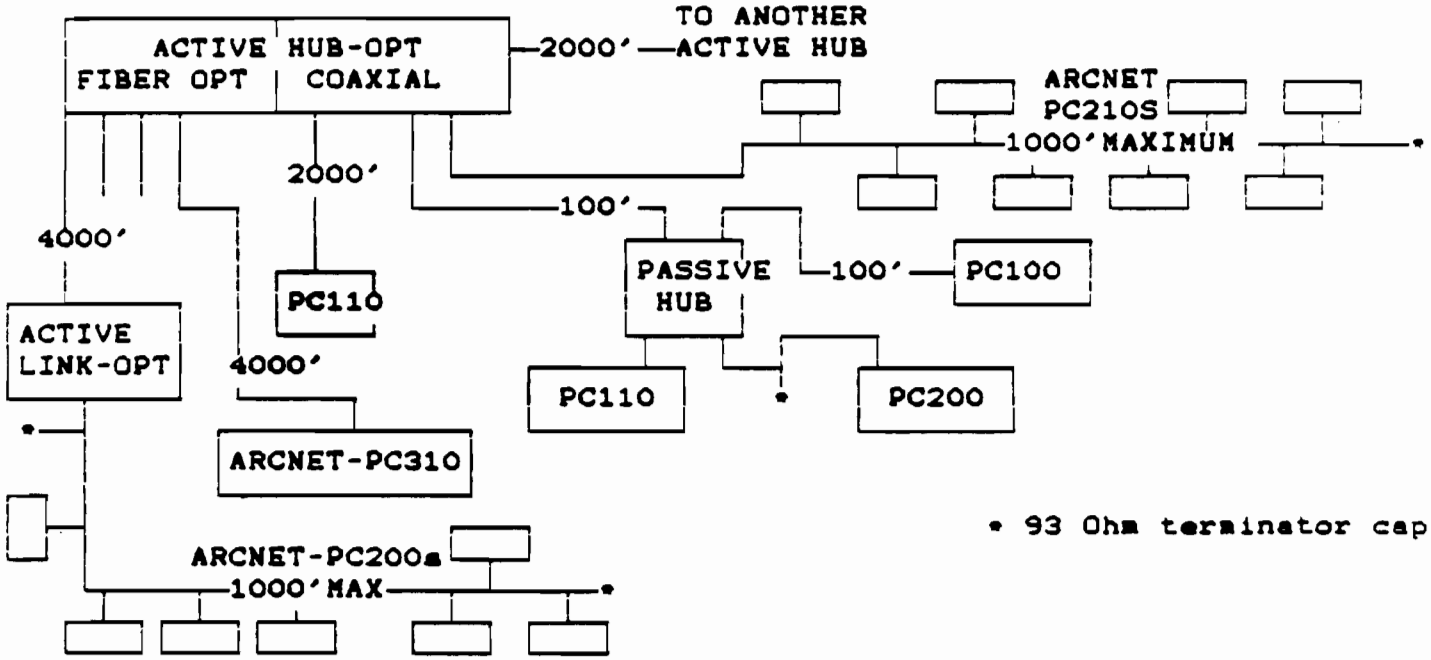
The ARCNET-PC 300, 310 are Fiber Optic ARCNET boards that can be used in a network with the following constraints:

1 Maximum distance is 4000 feet of 200 micron fiber optic cable.

2 To use with an existing ARCNET network, the ARCNET-PC 300,310 can be connected to either an SMC ACTIVE LINK-OPT for use with PC200,210 based system or an SMC ACTIVE HUB-OPT for use with multiple Fiber Optic ARCNET units.

2.3.4 TOPOLOGY EXAMPLE

The following example of a physical network layout is intended to demonstrate the interconnectability of SMC ARCNET:



3.0 ARCNET-PC SWITCH CONFIGURATION

3.1 SWITCH GROUPS OVERVIEW:

A switch is equivalent to logical 1 when rocker or slide is set to the down position and logical 0 when the rocker or slide is set to the up position. The switches within the Switch Group represent the binary equivalent of the address value required for proper software operation. Refer to your Software documentation for the proper address and interrupt values.

3.2 SWITCH GROUP #2 SETTINGS:

3.2.1 SWITCHES 1 - 8 NODE ADDRESS VALUE

All the switches in Switch Group #2 are used to set the station address. The station address value must be unique to each station. The LSB for the node address is switch 1.

EXAMPLE:

	switches 1 2 3 4 5 6 7 8	
SWITCH GROUP 2	U U - - U U U U - - D D - - - -	U = up, on, closed D = down, off, open

This setting has a value of 4 + 8 = 12 Decimal or 0C HEX for a station address or NODE ID of 0C.

3.3 SWITCH GROUP #1 SETTINGS:

3.3.1 SWITCHES 1 - 6 I/O ADDRESS VALUE

Switches 1-6 set the base I/O address whose value is 16 times the HEX value of the switches. The LSB for the I/O Address is switch 6.

EXAMPLE:

	switches 1 2 3 4 5 6	
SWITCH GROUP 1	- U - - - U D - D D D -	U = up, on, closed D = down, off, open

The value of the above setting is equal to 32 + 8 + 4 + 2 = 46 Decimal or 2E HEX which is used as a base I/O address of 2E0.

3.3.2 SWITCHES 7 - 10 RAM BUFFER ADDRESS VALUE

Switches 7-10 set the base address (segment) of the memory buffer whose value is 64 K [or 10000 HEX] times the value of the binary representation of the switches. The LSB for the Buffer Address is switch 10.

EXAMPLE:

	switches 7 8 9 10	
SWITCH GROUP 1	- - - U D D D -	U = up, on, closed D = down, off, open

The value of the above setting is equal to 8 + 4 + 2 = 14 Decimal or E HEX which is used as a RAM buffer address of E000:0

4.0 ARCNET-PC JUMPER CONFIGURATION

JUMPER PC100 TYPE	PC110 TYPE	FUNCTION
JP1	JP7	COM 9026 INTR = IRQ7
JP2	JP6	COM 9026 INTR = IRQ5
JP3	JP5	COM 9026 INTR = IRQ4
JP4	JP4	COM 9026 INTR = IRQ3
JP5	JP3	COM 9026 INTR = IRQ2
JP6*	JP2	COM 9026 ET2 (Normally open)
JP7*	JP1	COM 9026 ET1 (Normally open)

* Refer to Extended Timeout Function in Appendix A.0

5.0 ARCNET-PC REGISTERS

ADDRESS A3	A2	A1	A0	REGISTER
0	0	X	0	COM 9026 Interrupt Mask/Status Register
0	0	X	1	COM 9026 Command Register
1	0	X	X	ARCNET-PC Software Reset

X = Don't Care.

See Appendix A.0 COM 9026 Data Sheet for bit definitions of each register.

6.0 ARCNET-PC MEMORY ADDRESSING

ADDRESS A19	A18	A17	A16	A15	A14	MEMORY
X	X	X	X	0	0	2K X 8 Data Packet Buffer
X	X	X	X	1	0	8K X 8 Prom

Address bits A19 through A16 are selected by switches 7 through 10 in switch group 1 respectively.

7.0 THEORY OF OPERATION

While reading this section refer to Appendix C.0 - ARCNET-PC Block Diagram. For a detailed discussion of the COM 9026 refer to the data sheet in Appendix A.0.

7.1 Address Decoding

The ARCNET-PC family is an interface between the IBM Personal computer and the ARCNET modified token passing local area network. The on-board 2K X 8 data packet buffer and 8K X 8 prom are memory mapped in the control system's memory address space, whereas the COM 9026 registers and ARCNET-PC software reset function are IO mapped in the control systems IO address space. Address lines A19 through A16 compare with switches S1-7 through S1-10 to produce signal MREQ* when a processor cycle requests access to on-board ram or prom.

7.1 Address Decoding cont.

MREQ* is further decoded to produce signals RIM* to access the 9026, RAM* to access the additional 2K X 8 ram, and PROM* to access the 8K X 8 prom. The COM 9026 receives signal RIM* and produces all bus controlling signals to allow the processor synchronized access to the data packet buffer.

Address lines A9 through A4 compare with switches S1-1 to S1-6 to produce signal IOREQ* when a processor cycle requests access to a COM 9026 register, or wishes to perform an ARCNET-PC software reset. Signal IOREQ* is decoded further to produce signals RIOREQ* to access the COM 9026 registers and RESREQ* to access the ARCNET-PC software reset circuitry. The COM 9026 receives signal RIOREQ* and produces all bus controlling signals to allow the processor synchronized access to COM 9026 registers. RESREQ* enables a one-shot timer, of approximately 200 milliseconds, to reset the COM 9026 and COM 9032 under software control. While RESREQ* is active, the processor should not try to access COM 9026 Registers or the Data Packet Buffer.

7.2 Internal Address-Data Bus

All gating of address and data on the internal bus (IAI0 through IA8 and IAD7 through IAD0) is controlled by the COM 9026. For detailed timing specifications see appendix A.0. Signals ADIE* and ILE* allow chips A10 and A27 (74LS244) to gate lower address and data respectively onto the internal bus. Signals WAIT, R/W*, RIOREQ*, and RIM* allow data on the internal bus to be driven onto the IBM bus by A26 (74LS373). Signal AIE* allows address lines A10 through A8 to address the ram buffer.

7.3 Wait State Generator

The COM 9026 effects arbitration and synchronous access to the data packet buffer and COM 9026 registers through the use of the I/O CHRDY line. The COM 9026 asserts signal WAIT at the start of a processor 7.3 Wait State Generator cont.

access cycle to indicate it is not ready to transfer data. WAIT asserts I/O CHRDY to produce processor wait cycles. Signals IOREQ* and MREQ* using A8 (74LS175), A1 (74LS00), and A-25 (7406) assure proper synchronizing of the I/O CHRDY signal. The COM 9026 returns WAIT to its inactive state when it is ready for the processor to complete its cycle.

7.4 Interrupts

The ARCNET-PC Interrupt Circuit consists of jumpers JP1 through JP7, and elements of A24 (74LS244). The COM 9026 is capable of asserting signal INTR when certain status bits become true. A write to the COM 9026 MASK register specifies which status bits can generate the interrupt. Jumpers JP1 through JP5 connect signal INTR to interrupt lines IRQ7 and IRQ5 through IRQ2.

7.5 Cable Transceiver

The cable transceiver consists of the COM 9032, either the SMC HYC9058 or SMC HYC9068 hybird coaxial driver, and BNC connector J1. The cable transceivers function is to convert TX pulses from the COM 9026 to a format required by Datapoint ARCNET local area network specifications, and also to convert signals from the cable to NRZ data required by the COM 9026 RX input. The Datapoint ARCNET implementation uses a baseband system with RG62/U (93 ohm) coax. For a detailed discussion of this implementation, see Appendix B.0.

8.0 PROGRAMMING CONSIDERATIONS

For a description of basic COM 9026 programming considerations, refer to Technical Note TN5-2, Appendix B.0, section titled Programming the COM 9026.

When using the ARCNET-PC software reset function, an IO read or IO write to IO location XX8H, where XX values are determined by IO address selection switches, will produce approximately a 200 millisecond reset of the COM 9026 and COM 9032. During the time these devices are being reset, the processor should not access COM 9026 registers or the Data Packet Buffer.

STANDARD MICROSYSTEMS CORPORATION

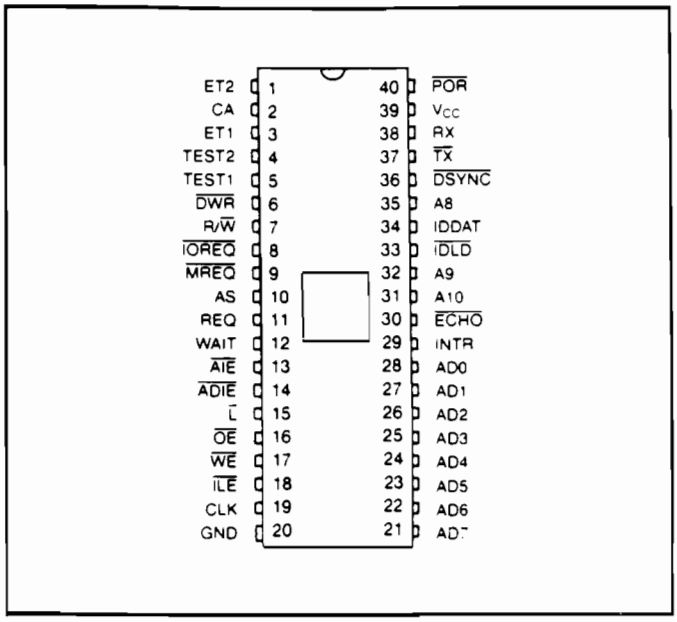
COM 9026

Local Area Network Controller LANC™

FEATURES

- 2.5 M bit data rate
- ARCNET* local area network controller
- Modified token passing protocol
- Self-reconfiguring as nodes are added or deleted from network
- Handles variable length data packets
- 16 bit CRC check and generation
- System efficiency increases with network loading
- Standard microprocessor interface
- Supports up to 255 nodes per network segment
- Ability to interrupt processor at conclusion of commands
- Interfaces to an external 1K or 2K RAM buffer
- Arbitrates buffer accesses between processor and COM 9026
- Replaces over 100 MSI/SSI parts
- Ability to transmit broadcast messages
- Compatible with broadband or baseband systems
- Compatible with any interconnect media (twisted pair, coax, etc.)

PIN CONFIGURATION



- Arbitrary network configurations can be used (star, tree, etc.)
- Single +5 volt supply

GENERAL DESCRIPTION

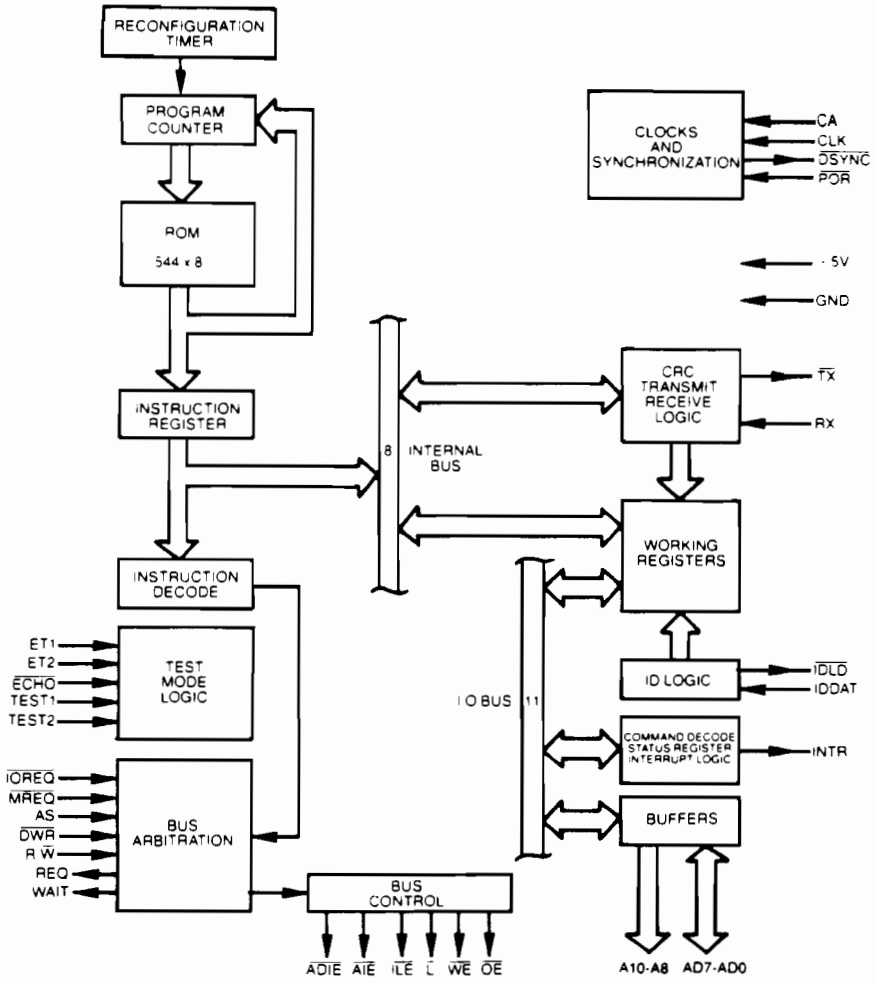
The COM 9026 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The COM 9026 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 9026 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 9026 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 9026 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 9026. The processor can write commands to the COM 9026 and also read COM 9026 status. The COM 9026 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

*ARCNET is a registered trademark of the Datapoint Corporation.



COM 9026 BLOCK DIAGRAM

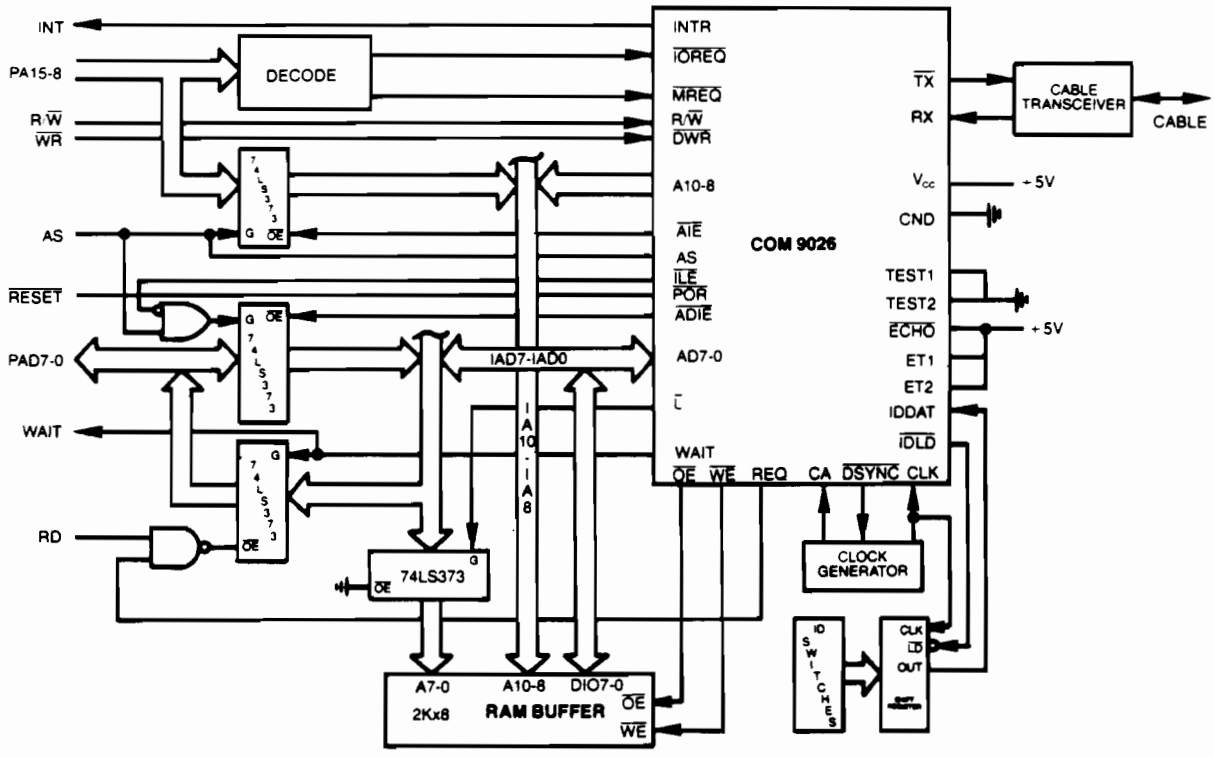


FIGURE 2—TYPICAL COM 9026 INTERFACE

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

PIN NO.	NAME	SYMBOL	FUNCTION
31, 32, 35	ADDRESS 10, 9, 8	A10, A9, A8	These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 9026 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected.
21, 22, 23, 24, 25, 26, 27, 28	ADDRESS DATA 7-0	AD7-AD0	These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 9026. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 9026.
8	I/O REQUEST	$\overline{IOREQ}$	This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 9026. This signal is sampled internally on the falling edge of AS.
9	MEMORY REQUEST	$\overline{MREQ}$	This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS.
7	READ/$\overline{WRITE}$	R/$\overline{W}$	A high level on this input signal indicates that the processor's access cycle to the COM 9026 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 9026. The write cycle will not be completed, however, until the $\overline{DWR}$ input is asserted. This signal is an internal transparent latch gated with AS.
10	ADDRESS STROBE	AS	This input signal is used by the COM 9026 to sample the state of the $\overline{IOREQ}$, $\overline{MREQ}$ and R/$\overline{W}$ inputs. The COM 9026 bus arbitration is initiated on the falling edge of this signal.
11	REQUEST	REQ	This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{MREQ}$ or $\overline{IOREQ}$ passed through an internal transparent latch gated with AS.
12	WAIT	WAIT	This output signal is asserted by the COM 9026 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 9026 is ready for the processor to complete its cycle.
6	DELAYED WRITE	$\overline{DWR}$	This input signal informs the COM 9026 that valid data is present on the processor's data bus for write cycles. The COM 9026 will remain in the WAIT state until this signal is asserted. $\overline{DWR}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded.
29	INTERRUPT REQUEST	INTR	This output signal is asserted when an enabled interrupt condition has occured. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
18	INTERFACE LATCH ENABLE	$\overline{ILE}$	This output signal, in conjunction with $\overline{ADIE}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address/data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 9026 operation.
14	ADDRESS/ DATA INPUT ENABLE	$\overline{ADIE}$	This output signal enables the processor's address/data bus (PAD7-PAD0) captured by AS or $\overline{ILE}$ onto the interface address/data bus (IAD7-IAD0).
13	ADDRESS INPUT ENABLE	$\overline{AIE}$	This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8).
15	LATCH	$\overline{L}$	This output signal latches the interface address/data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles.
17	WRITE ENABLE	$\overline{WE}$	This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{WE}$.
16	OUTPUT ENABLE	$\overline{OE}$	This output signal enables the RAM buffer output data onto the interface address/data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations.
33	ID LOAD	$\overline{IDLD}$	This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 9026. The shift register is clocked with the same signal that feeds the COM 9026 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 19.
34	ID DATA IN	IDDAT	This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1".
1, 3	EXTENDED TIMEOUT FUNCTION 2, 1	ET2, ET1	The levels on these two input pins specify the timeout durations used by the COM 9026 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details.
37	TRANSMIT DATA	$\overline{TX}$	This output signal contains the serial transmit data to the CABLE TRANSCEIVER.
38	RECEIVE DATA	RX	This input signal contains the serial receive data from the CABLE TRANSCEIVER.

DESCRIPTION OF PIN FUNCTIONS (Continued)

PIN NO.	NAME	SYMBOL	FUNCTION
4, 5	TEST PIN 2 TEST PIN 1	TEST2 TEST1	These input pins are grounded for normal chip operation. These pins are used in conjunction with ET2 and ET1 to enable various internal diagnostic functions when performing chip level testing.
30	ECHO DIAGNOSTIC ENABLE	$\overline{ECHO}$	When this input signal is low, the COM 9026 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal chip operation and is only utilized when performing chip level testing.
19	CLOCK	CLK	A continuous 5 MHz clock input used for timing of the COM 9026 bus cycles, bus arbitration, serial ID input, and the internal timers.
2	CA	CA	This input signal is a 5 MHz clock used to control the operation of the COM 9026 microcoded sequencer. This input is periodically halted in the high state by the $\overline{DSYNC}$ output.
36	DELAYED SYNC	$\overline{DSYNC}$	This output signal is asserted by the COM 9026 to cause the external clock generator logic to halt the CA clock. Refer to figure 9.
40	POWER ON RESET	$\overline{POR}$	This input signal clears the COM 9026 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network.
39	+5 VOLT SUPPLY	V_{CC}	Power Supply
20	GROUND	GND	Ground

PROTOCOL DESCRIPTION

LINE PROTOCOL DESCRIPTION

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte will take up exactly 11 clock intervals with a single clock interval being 400 nanoseconds in duration. As a result, 1 byte is transmitted every 4.4 microseconds and the time to transmit a message can be exactly determined. The line idles in a spacing (logic 0) condition. A logic '0' is defined as no line activity and a logic 1 is defined as a pulse of 200 nanoseconds duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic 1). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be sent as described below:

Invitations To Transmit

An ALERT BURST followed by three characters; an EOT (end of transmission—ASCII code 04 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to pass the token from one node to another.

Free Buffer Enquiries

An ALERT BURST followed by three characters; an ENQ (ENQuiry—ASCII code 05 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to ask another node if it is able to accept a packet of data.

Data Packets

An ALERT BURST followed by the following characters:

- — an SOH (start of header-ASCII code 01 HEX)
- —a SID (Source IDentification) character
- —two (repeated) DID (destination IDentification) characters.
- —a single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent.
- —N data bytes where COUNT = 256-N (512-N for a "long packet")
- —two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

Acknowledgements

An ALERT BURST followed by one character; an ACK (ACKnowledgement—ASCII code 06 HEX) character. This message is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES.

Negative Acknowledgements

An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement—ASCII code 15 HEX). This message is used as a negative response to FREE BUFFER ENQUIRIES.

NETWORK PROTOCOL DESCRIPTION

Communication on the network is based on a "modified token passing" protocol. A "modified token passing" scheme is one in which all token passes are acknowledged by the node receiving the token. Establishment of the network configuration and management of the network protocol are handled entirely by the COM 9026's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM 9026 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet.

If the packet is received successfully, the receiving node transmits an acknowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicating successful or unsucessful delivery of the packet. An interrupt mask permits the COM 9026 to generate an interrupt to the processor when selected status bits become true. Figure 3 is a flow chart illustrating the internal operation of the COM 9026.

NETWORK RECONFIGURATION

A significant advantage of the COM 9026 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated a NETWORK RECONFIGURATION is performed. When a new COM 9026 is turned on (creating a new active node on the network), or if the COM 9026 has not received an INVITATION TO TRANSMIT for 840 milliseconds, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM 9026 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM 9026 sees an idle line for greater than 78.2 microseconds, which will only occur when the token is lost, each COM 9026 starts an internal time out equal to 146 microseconds times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM 9026 starts sending INVITATIONS TO TRANSMIT with the DID equal to the currently stored NID. Within a given network, only one COM 9026 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM 9026 waits for activity on the line. If there is no activity for 74.7 microseconds, the COM 9026 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 microsecond timeout expires, the COM 9026 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM 9026 on the network will finally have saved a NID value equal to the ID of the COM 9026 that assumed control from it. From then until the next NETWORK RECONFIGURATION, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT sent to ID's not on the network. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will time out and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes and the highest ID number on network but will be in the range of 24 to 61 milliseconds.

BROADCAST MESSAGES

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the destination ID (DID) equal to zero. Figure 8 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most signficant bit of the ENABLE RECEIVE TO PAGE nn command (see "WRITE COM 9026 COMMANDS") to a logic zero.

COM 9026 OPERATION

BUFFER CONFIGURATION

During a transmit sequence, the COM 9026 fetches data from the Transmit Buffer, a 256 (or 512) byte segment of the RAM buffer. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM 9026 will interpret the packet as a long or short packet depending on whether the contents of buffer location 02 is zero or non zero. During a receive sequence, the COM 9026 stores data in the receive buffer, also a 256 (or 512) byte segment of the RAM buffer. The processor I/O command which enables either the COM 9026 receiver or the COM 9026 transmitter also initializes the respective buffer page register. The formats of the buffers (both 256 and 512 byte) are shown below.

FIGURE 8— RAM BUFFER PACKET CONFIGURATION

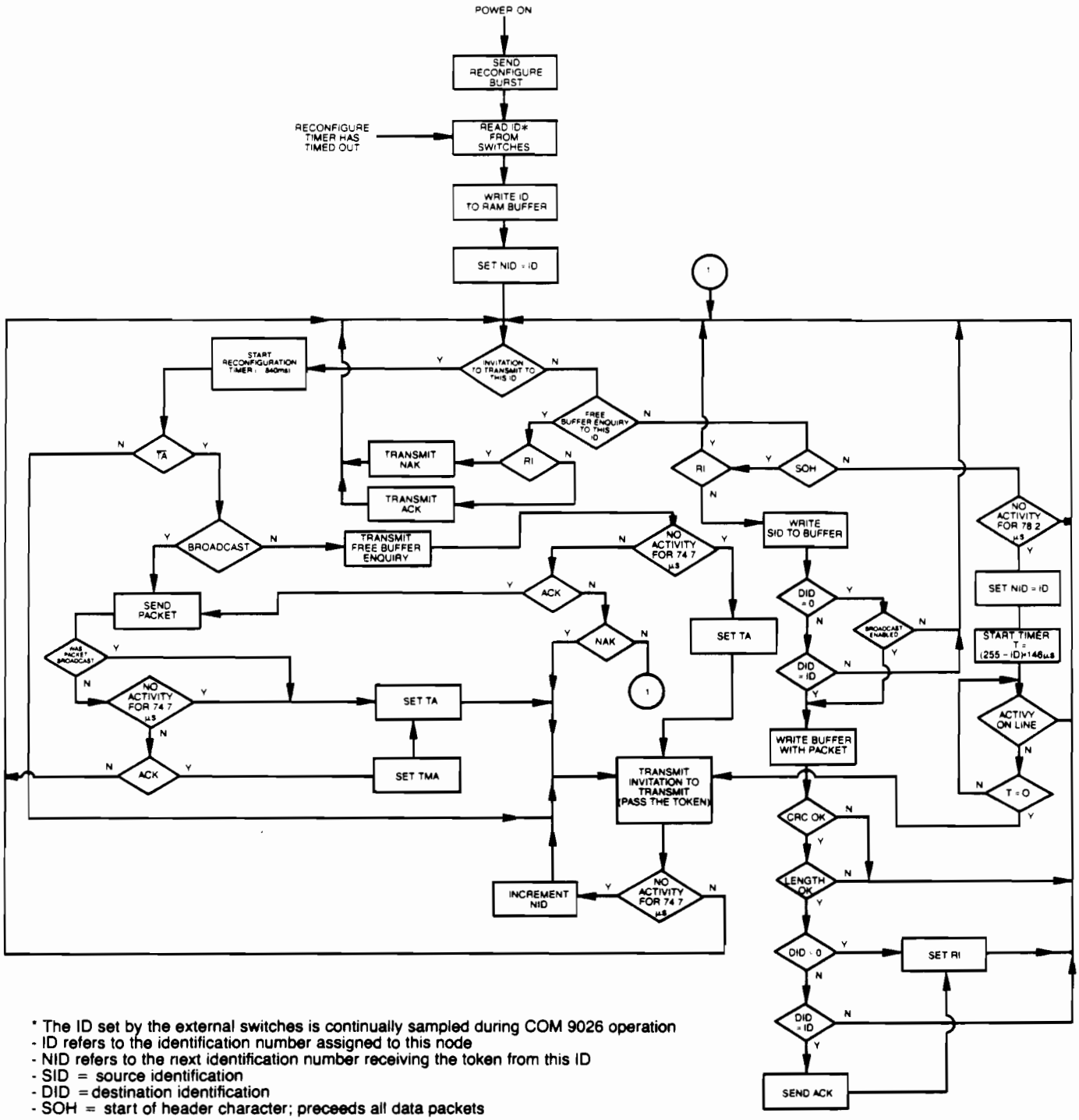
ADDRESS	FORMAT
0	SID
1	DID
2	COUNT = 256 - N
	NOT USED
COUNT	DATA BYTE 1
	DATA BYTE 2
	•
	•
	•
	DATA BYTE N-1
255	DATA BYTE N
	NOT USED
511	

SHORT PACKET (256 OR 512 BYTE PAGE)

ADDRESS	FORMAT
0	SID
1	DID
2	0
3	COUNT = 512 - N
	NOT USED
COUNT	DATA BYTE 1
	DATA BYTE 2
	•
	•
	•
	DATA BYTE N-1
511	DATA BYTE N

LONG PACKET (512 BYTE PAGE)

N = DATA PACKET LENGTH
SID = SOURCE ID
DID = DESTINATION ID (0 FOR BROADCASTS)



* The ID set by the external switches is continually sampled during COM 9026 operation
- ID refers to the identification number assigned to this node
- NID refers to the next identification number receiving the token from this ID
- SID = source identification
- DID = destination identification
- SOH = start of header character; preceeds all data packets

FIGURE 3—9026 OPERATION

PROCESSOR INTERFACE

Figure 2 illustrates a typical COM 9026 to processor interface. The signals on the left side of this figure represent typical processor signals with a 16 bit address bus and an 8 bit data bus with the data bus multiplexed onto the lower 8 address lines (PAD7-PAD0). The processor sees a network node (a node consists of a COM 9026, RAM buffer, cable transceiver, etc. as shown in figure 2) as 2K memory locations and 4 I/O locations within the COM 9026.

The RAM buffer is used to hold data packets temporarily prior to transmission on the network and as temporary storage of all received data packets directed to the particular node. The size of the buffer can be as large as 2K byte locations providing four pages at a maximum of 512 bytes per page. For packet lengths smaller than 256 bytes, a 1K RAM buffer can be used to provide four pages of storage. In this case address line IA8 (sourced from either the COM 9026 or the processor) should be left unconnected. Since four pages of RAM buffer are provided, both transmit and receive operations can be double buffered with respect to the processor. For instance, after one data packet has been loaded into a particular page within the RAM buffer and a transmit command for that page has been issued, the processor can start loading another page with the next message in a multimessage transmission sequence. Similarly, after one message is received and completely loaded into one page of the RAM buffer by the COM 9026, another receive command can be issued to allow reception of the next packet while the first packet is read by the processor. In general, the four pages in the RAM buffer can be used for transmit or receive in any combination. In addition, the processor will also use the interface bus (IA10-IA8, IAD7-IAD0) when performing I/O access cycles (status reads from the COM 9026 or command writes to the COM 9026).

To accomplish this double buffering scheme, the RAM buffer must behave as a dual port memory. To allow this RAM to be a standard component, arbitration and control on the interface bus (IA10-IA8, IAD7-IAD0) is required to permit both the COM 9026 and the processor access to the RAM buffer and, at the same time, permit all processor I/O operations to or from the COM 9026.

Processor access cycle requests begin on the trailing edge of AS if either $\overline{\text{IOREQ}}$ or $\overline{\text{MREQ}}$ is asserted. These access cycles run completely asynchronous with respect to the COM 9026. Because of this, upon processor access cycle requests, the COM 9026 immediately puts the processor into a wait state by asserting the WAIT output. This gives the COM 9026 the ability to synchronize and control the processor access cycle. When the processor access cycle is synchronized by the COM 9026, the WAIT signal is eventually removed allowing the processor to complete its cycle.

For processor RAM buffer access cycles, $\overline{\text{AIE}}$ and $\overline{\text{ADIE}}$ enable the processor address captured during AS time onto the interface address bus (IA10-IA8, IAD7-IAD0). The signal $\overline{\text{L}}$ will capture the 8 least significant bits of this address (appearing on IAD7-IAD0) before the data is multiplexed onto it. At the falling edge of L, a stable address is presented to the RAM buffer. For read cycles, $\overline{\text{OE}}$ allows the addressed RAM buffer data to source the interface address/data bus (IAD7-IAD0). In figure 2, this information is passed into a transparent latch gated with WAIT. At the falling edge of WAIT, the data accessed by the processor is captured

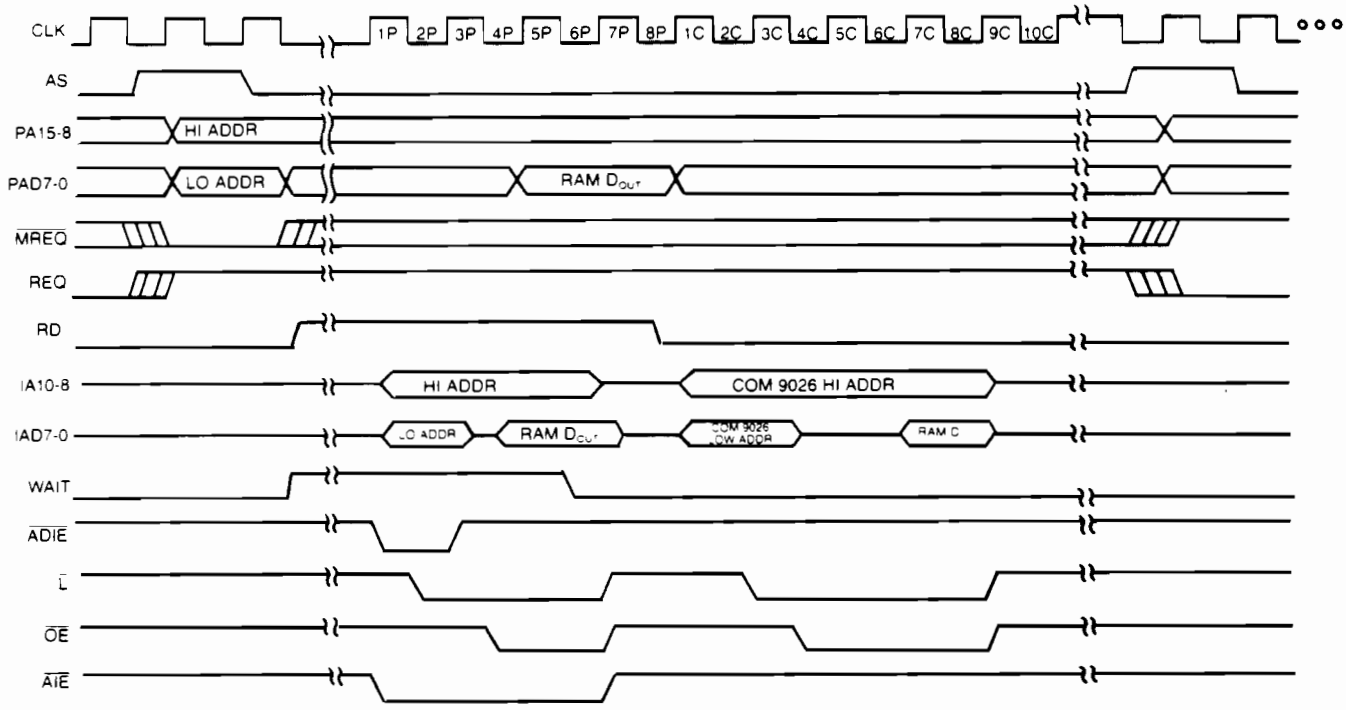


FIGURE 4—PROCESSOR READ RAM FOLLOWED BY COM 9026 READ RAM

and driven out via the logic function RD anded with REQ. For processor I/O read cycles from the COM 9026, ADIE and AIE are used to enable the processor address into the COM 9026. Data out of the COM 9026 is gated through the transparent latch and appears on the processor's data bus with the same control signals used for RAM read cycles.

For processor write cycles, after the falling edge of L, the COM 9026 produces a WE (write enable) output to the RAM buffer, and the ILE output from the COM 9026 allows the processor data to source the interface address/data bus (IAD7-IAD0). At this time the COM 9026 waits for DWR before concluding the cycle by removing the WAIT output. DWR should only be used if the processor cannot deliver the data to be written in enough time to satisfy the write setup time requirements of the RAM buffer. By delaying the activation of DWR, the period of the write cycle will be extended until the write data is valid. Since the architecture and operation of the COM 9026 requires periodic reading and writing of the RAM buffer in a timely manner, holding the DWR input off for a long period of time, or likewise by running the processor at a slow speed, can result in a data overflow condition. It is therefore recommended that if the processor write data setup time to the RAM buffer is met, then the DWR input should be grounded.

For processor I/O write cycles to the COM 9026, ADIE and AIE are used to enable the processor's address onto the interface data bus. ILE is used to enable the processor's write data into the COM 9026. Delaying the activation of DWR will hold up the COM 9026 cycle requiring the same precautions as stated for Processor RAM Write cycles.

As stated previously, processor requests occur at the falling edge of AS if either IOREQ or MREQ are active. COM 9026 requests occur when the transmitter or receiver need to read or write the RAM buffer in the course of executing the command. If the COM 9026 requests a bus cycle at the same time as the processor, or shortly after the processor, the COM 9026 cycle will follow immediately after the processor cycle. Figure 4 illustrates the timing relationship of a Processor RAM Read cycle followed by a COM 9026 RAM read cycle. Once the AS signal captures the processor address to the RAM buffer and requests a bus cycle, it takes 4 CLK periods for the processor cycle to end. Figure 4 breaks up these 4 CLK periods into 8 half clock interval labeled 1P through 8P. A COM 9026 access cycle will take 5 CLK periods to end. Figure 4 breaks up these 5 CLK periods into 10 half intervals labeled 1C through 10C.

If a processor cycle request occurs after a COM 9026 request has already been granted, the COM 9026 cycle will occur first, as shown in figure 5. Figure 5 illustrates the timing relationship of a COM 9026 RAM Write cycle followed by a Processor RAM Write cycle. Due to the asynchronous nature of the bus requests (AS and CLK), the transition from the end of the COM 9026 cycle to the beginning of the processor cycle might have some dead time. Refering to figure 5, if AS falling edge occurs after the start of half CLK interval 9C, no real contention exists and it will take between 200 and 500 nanoseconds before the processor cycle can start. The start of the processor cycle is defined as the time when the COM 9026 produces a leading edge on both ADIE and AIE. If the processor request occurs before the end of half

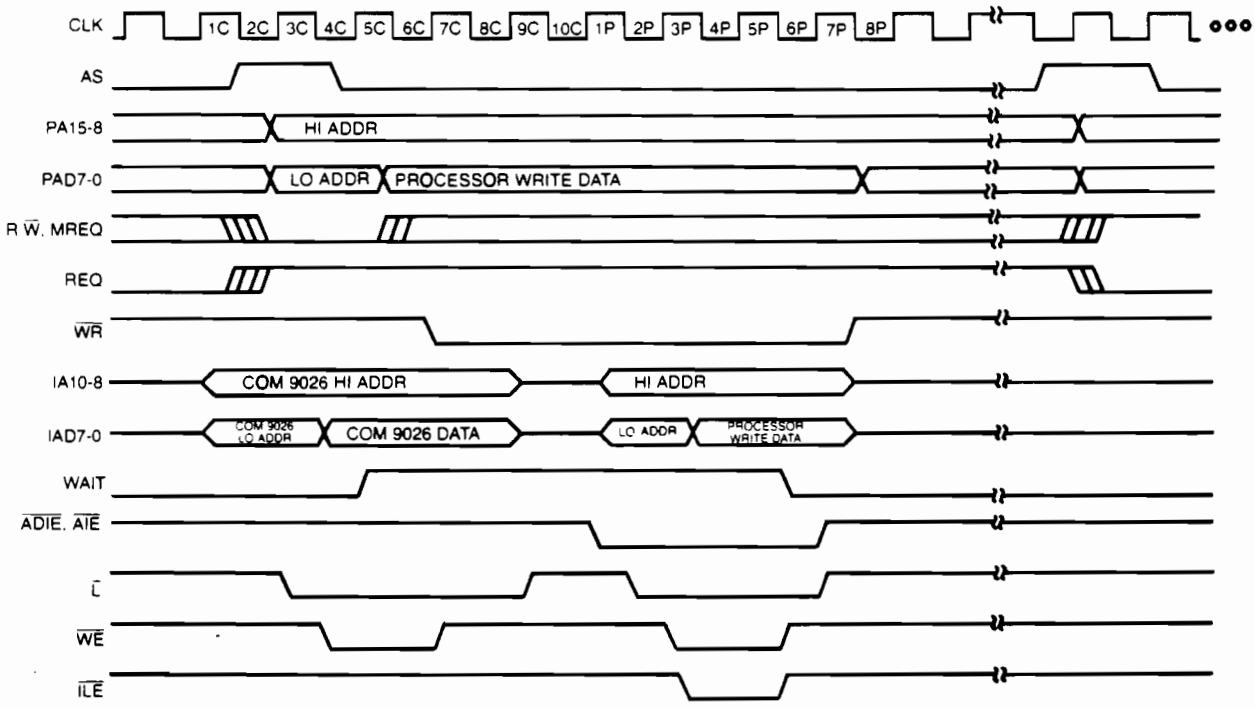


FIGURE 5—COM 9026 WRITE RAM FOLLOWED BY PROCESSOR WRITE RAM

CLK interval 5C (figure 5 illustrates this situation), then the processor cycle will always start at half CLK interval 1P. The uncertainty is introduced when the processor request occurs during half CLK intervals 6C, 7C or 8C. In this case, the processor cycle will start between 200 and 500 nanoseconds later depending on the particular timing relation between AS and CLK. The maximum time between processor request and processor cycle start, which occurs when the processor request comes just after a COM 9026 request, is 1300 nanoseconds. It should be noted that all times specified above assume a nominal CLK period of 200 nanoseconds.

Figures 6 and 7 illustrate timing for Processor Read COM 9026 and Processor Write COM 9026 respectively. These cycles are also shown divided into 8 half clock intervals (1P through 8P) and can be inserted within figures 4 and 5 if these processor cycles occur.

POWER UP AND INITIALIZATION

The COM has the following power up requirements:

1—The $\overline{POR}$ input must be active for at least 100 milliseconds.
2—The CLK input must run for at least 10 clock cycles before the $\overline{POR}$ input is removed.
3—While $\overline{POR}$ is asserted, the CA input may be running or held high. If the CA input is running, $\overline{POR}$ may be released asynchronously with respect to CA. If the CA input is held high, $\overline{POR}$ may be released before CA begins running.

During $\overline{POR}$ the status register will assume the following state:

BIT 7 (RI) set to a logic "1".
BIT 6 (ETS2) not affected
BIT 5 (ETS1) not affected
BIT 4 (POR) set to a logic "1".
BIT 3 (TEST) set to a logic "0".
BIT 2 (RECON) set to a logic "0".
BIT 1 (TMA) set to a logic "0".
BIT 0 (TA) set to a logic "1".

In addition the $\overline{DSYNC}$ output is reset inactive high and the interrupt mask register is reset (no maskable interrupts enabled). Page 00 is selected for both the receive and the transmit RAM buffer. After the $\overline{POR}$ signal is removed, the COM 9026 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM 9026 will start operation four CA clock cycles after the $\overline{POR}$ signal is removed. At this time, the COM 9026, after reading its ID from the external shift register, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number as previously read from the external shift register. The processor may then read RAM buffer address 01 to determine the COM 9026 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

CLOCK GENERATOR

The COM 9026 uses two separate clock inputs namely CA and CLK. The CLK input is a 5 MHz free running clock and the CA input is a start/stop clock periodically stopped and started to allow the COM 9026 to synchronize to the incoming data that appears on the RX input.

Figure 9 illustrates the timing of the CA clock generator and its relationship to the $\overline{DSYNC}$ output and the RX input. The $\overline{DSYNC}$ output is used to control the stopping of the CA clock. On the next rising edge of the CA input after $\overline{DSYNC}$ is asserted, CA will remain in the high state. The CA clock remains halted in the high state as long as the RX signal remains high. When the RX signal goes low, the CA clock is restarted and remains running until the next falling edge of $\overline{DSYNC}$. (See figure 20 for an implementation of this circuit.)

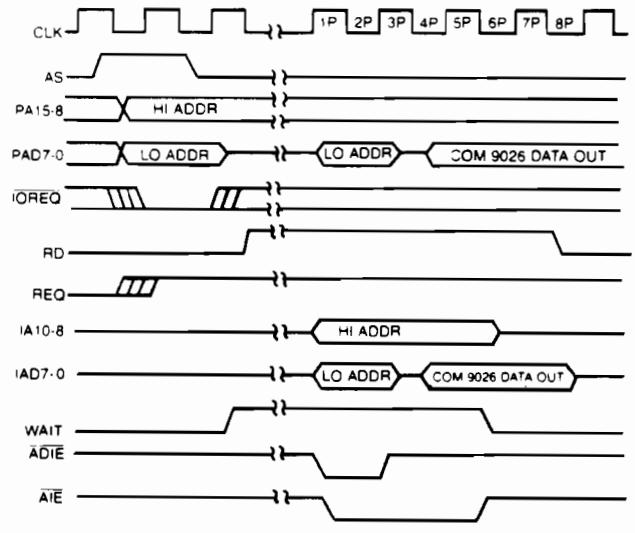


FIGURE 6—PROCESSOR READ COM 9026

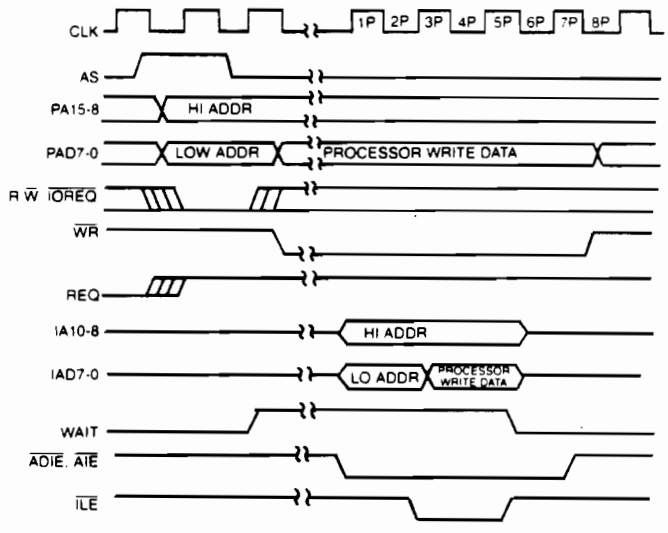


FIGURE 7—PROCESSOR WRITE COM 9026

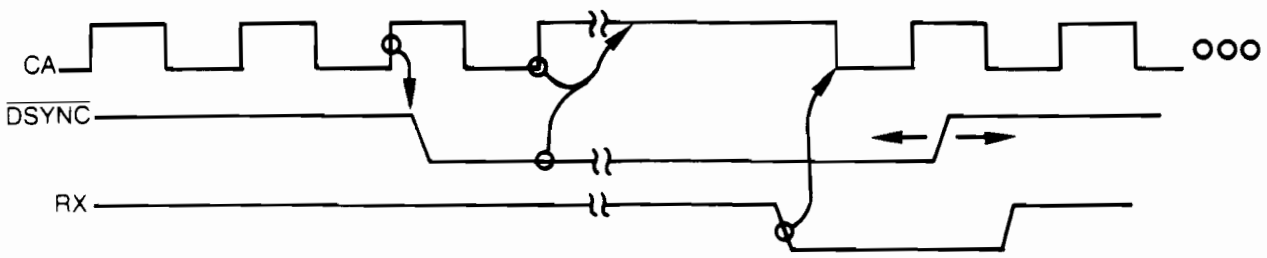


FIGURE 9—CA CLOCK GENERATOR TIMING

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM 9026 operation.

Response Time

This timeout is equal to the round trip propagation delay between the 2 furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM 9026 to start sending a message in response to a received message) which is known to be 12 microseconds. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 microseconds translates to a distance of about 4 miles. The flow chart in figure 3 uses a value of 74.7 microseconds (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

This time is associated with a NETWORK RECONFIGURATION. Refering to figure 3, during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 microseconds. This 78 microsecond is equal to the response time of 74.7 microseconds plus the time it takes the COM 9026 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 microseconds to allow for margin.

Reconfiguration Time

If any node does not receive the token within this time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM 9026 can operate by controlling the 3 timeout values described above. Table 1 illustrates the response time and reconfiguration time as a function of the ET2 and ET1 inputs. The idle time will always be equal to the response time plus 3.5 microseconds. It should be noted that for proper network operation, all COM 9026's connected to the same network must have the same response time, idle time and reconfiguration time.

ET2	ET1	RESPONSE TIME (μs)	RECONFIGURATION TIME (ms)
1	1	74.7	840
1	0	283.4	1680
0	1	561.8	1680
0	0	1118.6	1680

TABLE 1
COM 9026 INTERNAL PROGRAMMABLE TIMER VALUES

I/O COMMANDS

I/O commands are executed by activating the $\overline{IOREQ}$ input. The COM 9026 will interrogate the AD0 and the R $\overline{W}$ inputs at the AS time to execute commands according to the following table:

$\overline{IOREQ}$	AD0	R/$\overline{W}$	FUNCTION
low	low	low	write interrupt mask
low	low	high	read status register
low	high	low	write COM 9026 command
low	high	high	reserved for future use

READ STATUS REGISTER

Execution of this command places the contents of the status register on the data bus (AD7-AD0) during the read portion of the processor's read cycle. The COM 9026 status register contents are defined as follows:

BIT 7—Receiver inhibited (RI)—This bit, if set high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. The setting of this bit can cause an interrupt via INTR if enabled during a WRITE INTERRUPT MASK command. No messages will be received until an ENABLE RECEIVE TO PAGE nn command is issued. After any message is received, the receiver is automatically inhibited by setting this bit to a logic one.

BIT 6—Extended Timeout Status 2 (ETS2)—This bit reflects the current logic value tied to the ET2 input pin (pin 1).

BIT 5—Extended Timeout Status 1 (ETS1)—This bit reflects the current logic value tied to the ET1 input pin (pin 3).

BIT 4—Power On Reset (POR)—This bit, if set high, indicates that the COM 9026 has received an active signal on the $\overline{POR}$ input (pin 40). The setting of this bit will cause a nonmaskable interrupt via INTR.

BIT 3—Test (TEST)—This bit is intended for test and diagnostic purposes. It will be a logic zero under any normal operating conditions.

BIT 2—Reconfiguration (RECON)—This bit, if set high, indicates that the reconfiguration timer has timed out because the RX input was idle for 78.2 microseconds. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command. The bit is reset low during a CLEAR FLAGS command.

BIT 1—Transmit Message Acknowledged (TMA)—This bit, if set high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast mesages are never acknowledged.

BIT 0—Transmitter Available (TA)—This bit, if set high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of a ENABLE TRANSMIT FROM PAGE nn command or upon the execution of a DISABLE TRANSMITTER command. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command.

WRITE INTERRUPT MASK

The COM 9026 is capable of generating an interrupt signal when certain status bits become true. A write to the MASK register specifies which status bits can generate the interrupt. The bit positions in the MASK register are in the same position as their corresponding status bits in the STATUS register with a logic one in a bit position enabling the corresponding interrupt. The setting of the TMA, EST1, and EST2 status bits will never cause an interrupt. The POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding MASK register bit. The MASK register takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	XXX	XXX	XXX	XXX	RECON TIMER	XXX	TRANSMITTER AVAILABLE

The three maskable status bits are anded with their respective mask bits, and the results, along with the POR status bit, are or'ed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when the interrupting status bit is reset to a logic "0" or when the corresponding bit in the MASK register is reset to a logic "0". To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding masks bits should be reset to a logic zero.

WRITE COM 9026 COMMANDS

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the following commands:

WRITTEN DATA	COMMAND
00000000	reserved for future use
00000001	DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission has not yet started) when the COM 9026 next receives the token. This command will set the TA (Transmitter Available) status bit when the token is received.
00000010	DISABLE RECEIVER—This command will cancel any pending receive command. If the COM 9026 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000nn011	ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM 9026 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are set to a logic "0". The TA bit is set to a logic one upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM 9026 has received an acknowledgement from the destination COM 9026. This acknowledgement is strictly hardware level which is sent by the receiving COM 9026 before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors, etc. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 3 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00nn100	ENABLE RECEIVE TO PAGE nn—This command allows the COM 9026 to receive data packets into RAM buffer page nn and sets the RI status bit to a logic zero. If "b" is a logic "1", the COM 9026 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to a logic one upon successful reception of a message.
0000c101	DEFINE CONFIGURATION—If c is a logic "1", the COM 9026 will handle short as well as long packets. If c is a logic "0", the COM 9026 will only handle short packets (less than 254 bytes).
000rp110	CLEAR FLAGS—If p is a logic "1" the POR status flag is cleared. If r is a logic "l", the RECON status flag is cleared.

All other combinations of written data are not permitted and can result in incorrect chip and/or network operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0 to 70°C
Storage Temperature Range	−55 to 150°C
Lead Temperature (soldering, 10 seconds)	+325°C
Positive Voltage on any pin	+8V
Negative Voltage on any pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	input low voltage	−0.3		0.8	V	
V_{IH1}	input high voltage 1	2.2		V_{CC}	V	except CA and CLK
V_{IH2}	input high voltage 2	V_{CC}−0.5		6.5	V	for CA or CLK
V_{OL1}	output low voltage 1			0.4	V	I_{OL} = 1.6 ma
V_{OL2}	output low voltage 2			0.5	V	I_{OL} = 2.0 ma
V_{OH}	output high voltage (1)	2.4			V	except $\overline{TX}$, DSYNC
I_L	input leakage current			±10	µA	
C_{IN}	input capacitance			20	pf	
C_{DB}	data bus capacitance			50	pf	
C_L	all other capacitance			30	pf	
I_{CC}	power supply current			350	ma	

V_{OH2} 3.2 $\overline{TX}$, DSYNC

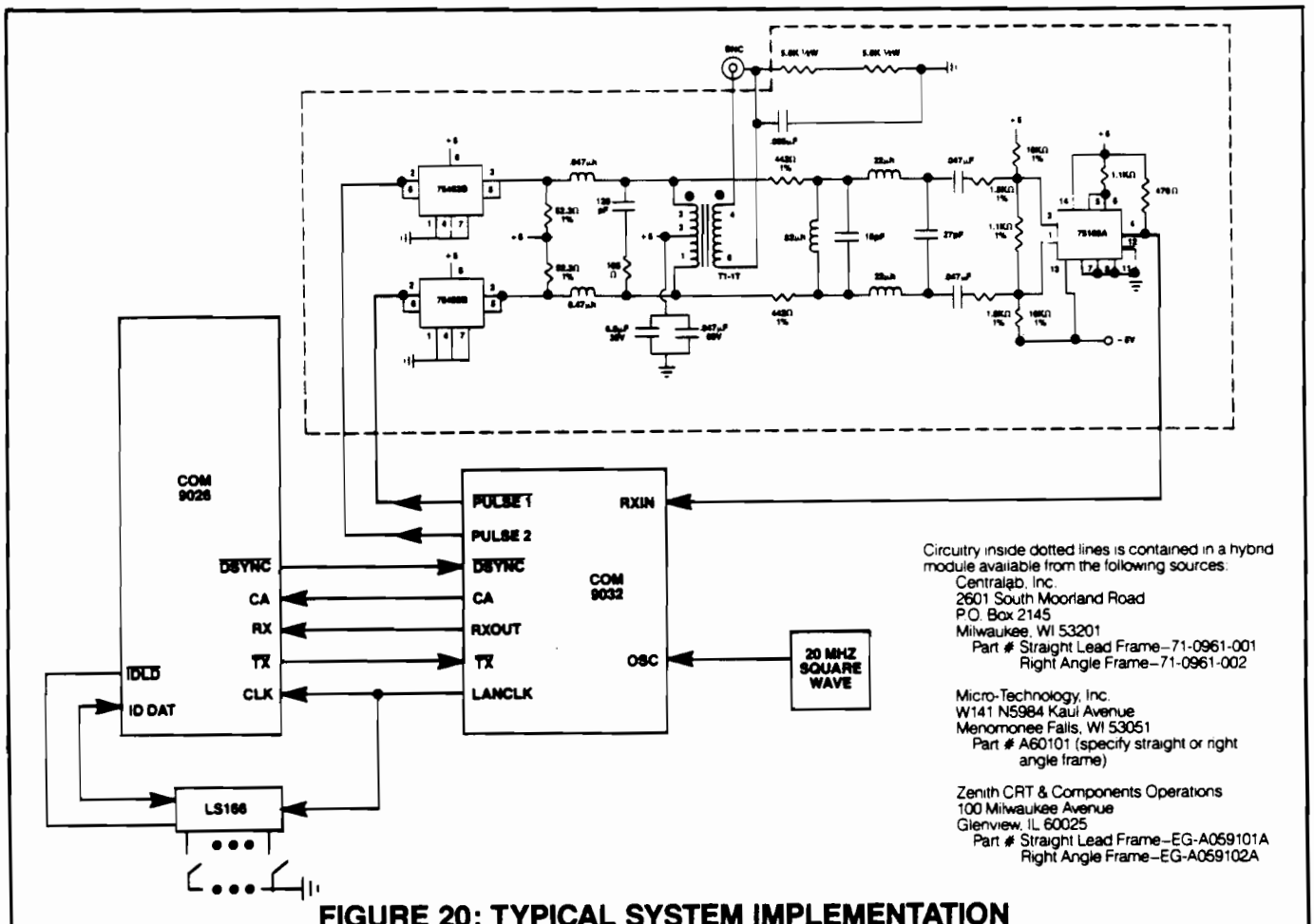


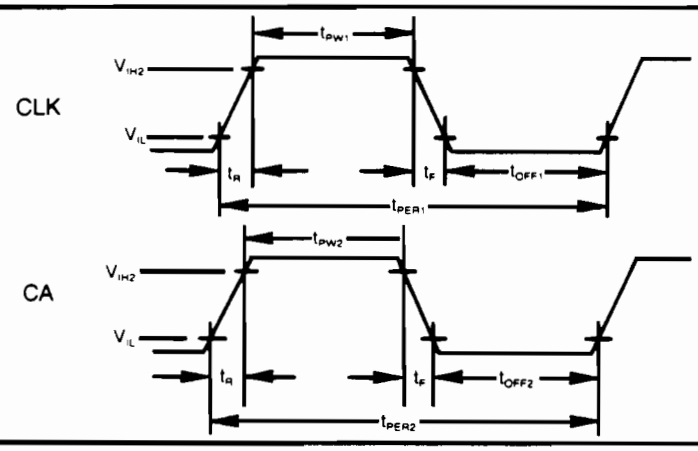
FIGURE 20: TYPICAL SYSTEM IMPLEMENTATION

AC ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0V ± 5%)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t_{PW1}	CLK pulse width	65			ns	
t_{PER1}	CLK period	190	200	600	ns	
t_{OFF1}	CLK off time	65			ns	
t_{PW2}	CA pulse width	60			ns	
t_{PER2}	CA period	190			ns	
t_{OFF2}	CA off time	60	100	300	ns	
t_R	CLK, CA rise time			20	ns	
t_F	CLK, CA fall time			20	ns	
t_1	width of addr. strobe	50			ns	
t_2	REQ output delay	0		100	ns	
t_3	WAIT assertion delay	0		200	ns	
t_4	delay to rising edge of processor cycle	t_P		$2t_P + 100$	ns	$t_P = t_{PER1}$
t_5	data hold into COM 9026	80			ns	
t_6	setup COM 9026 data out	60			ns	
t_7	$\overline{WE}$ delay from CLK	0		100	ns	
t_8	$\overline{TX}$ on delay from CA falling edge	10		150	ns	
t_9	$\overline{TX}$ off delay from CA rising edge	10		150	ns	
t_{10}	AS period	7/2 t_P			ns	$t_P = t_{PER2}$
t_{11}	$\overline{DSYNC}$ delay from CA rising edge	10		150	ns	
t_{12}	delay to wait off	20		100	ns	
t_{13}	$\overline{DWR}$ setup time	50			ns	
t_{14}	$\overline{ILE}$ delay from CLK	10		100	ns	
t_{15}	processor addr. setup from $\overline{ADIE}$,			50	ns	
t_{16}	processor command setup time	125			ns	
t_{17}	addr. enable setup time to $\overline{L}$	50			ns	
t_{18}	addr. hold time from $\overline{L}$	50			ns	
t_{19}	strobe and data hold for read	20			ns	
t_{20}	AD bus HI impedance to $\overline{OE}$s	0			ns	
t_{21}	delay of $\overline{IDLD}$ from CLK rising edge	0		120	ns	
t_{22}	delay of IDDAT from CLK rising edge	0		50	ns	
t_{23}	off delay from CLK rising edge	0		100	ns	
t_{24}	addr. to RAM data valid			300	ns	
t_{25}	$\overline{OE}$ setup to WAIT falling edge	140			ns	
t_{26}	strobe & data hold for write	50			ns	
t_{27}	addr. enable setup to WAIT	300			ns	
t_{28}	$\overline{ADIE}$ to $\overline{OE}$ delay	40			ns	
t_{29}	COM 9026 write data hold time	80			ns	
t_{30}	$\overline{OE}$ to RAM data valid	0		140	ns	
t_{31}	status setup to AS falling edge	50			ns	
t_{32}	status hold from AS falling edge	50			ns	
t_{33}	RX setup to CA rising edge	80			ns	
t_{34}	RX hold time from CA rising edge	30			ns	
t_{35}	$\overline{POR}$ active time	100			ms	after V_{cc} has been stable for time t_{35}, the minimum $\overline{POR}$ active time is 10 cycles of CLK.

The above timing information is valid for a worst case 40% to 60% duty cycle on CLK. All times are measured from the 50% point of the signals.

FIGURE 10—
CLK, CA
AC CHARACTERISTICS



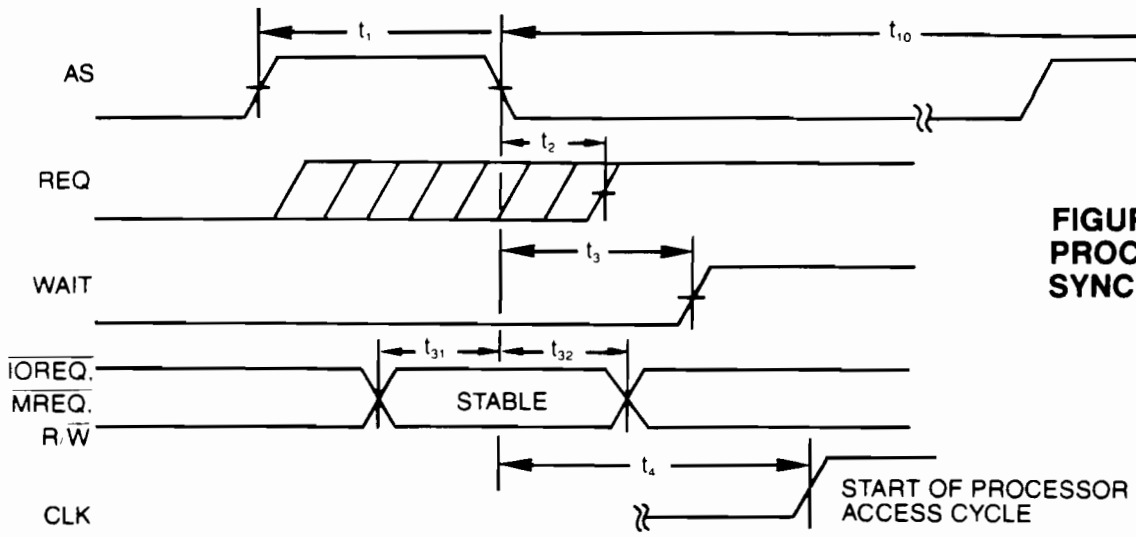


FIGURE 11—PROCESSOR ACCESS SYNCHRONIZATION

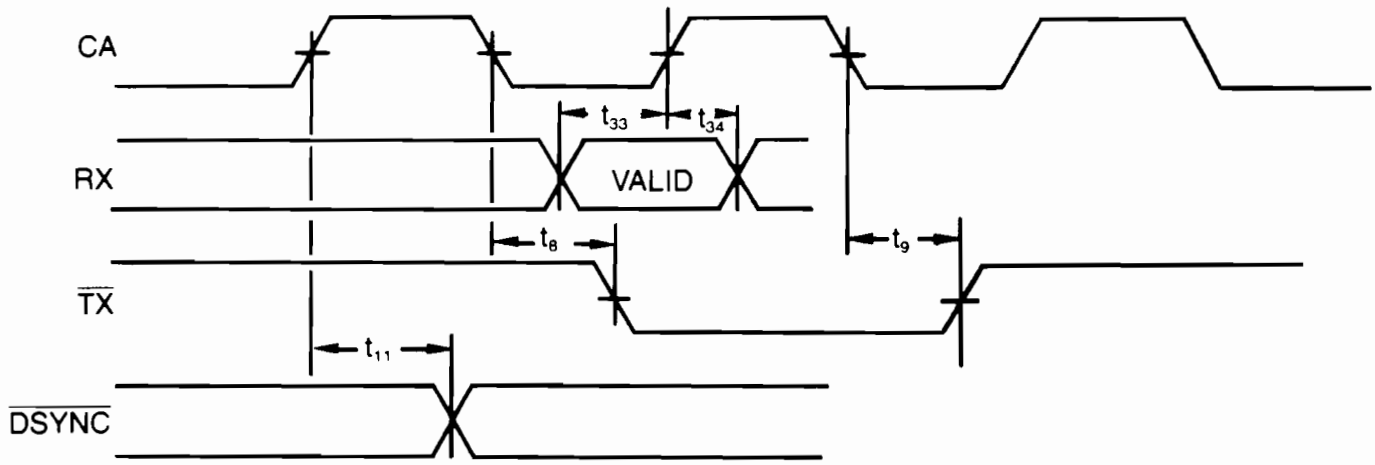


FIGURE 12—TRANSMIT AND RECEIVE TIMING

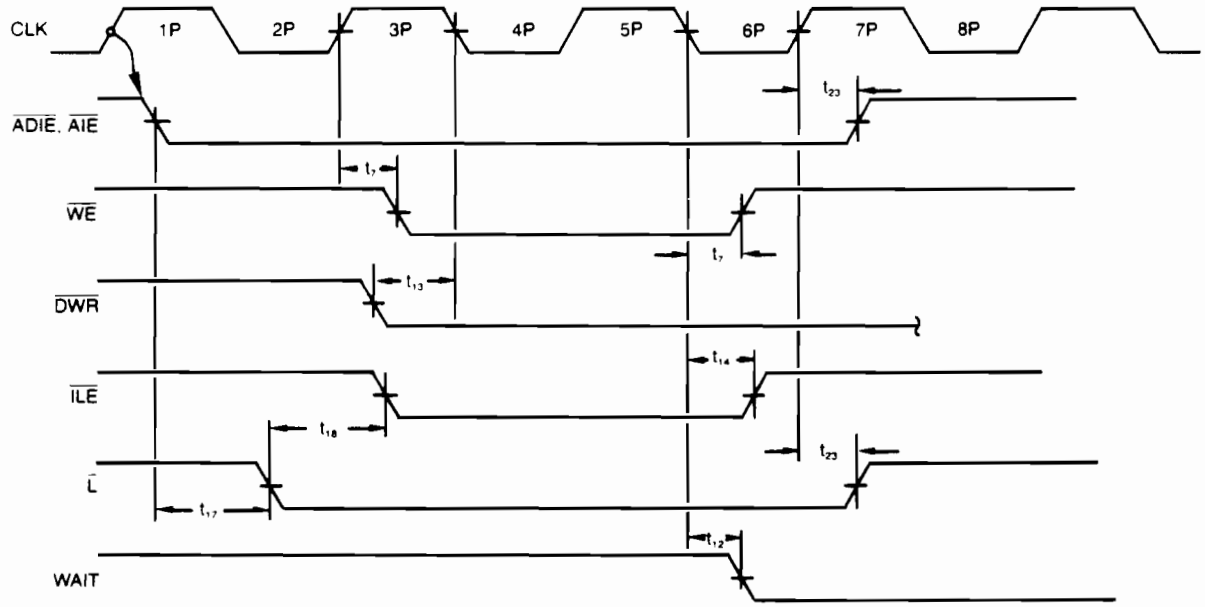


FIGURE 13—PROCESSOR WRITE RAM AC TIMING

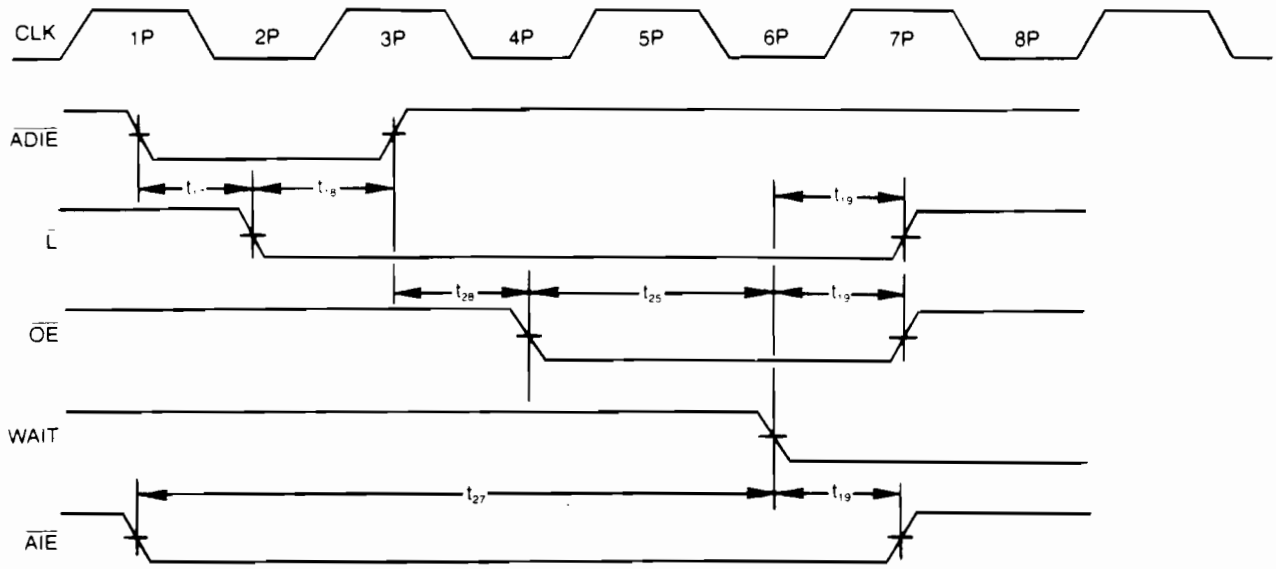


FIGURE 14—PROCESSOR READ RAM AC TIMING

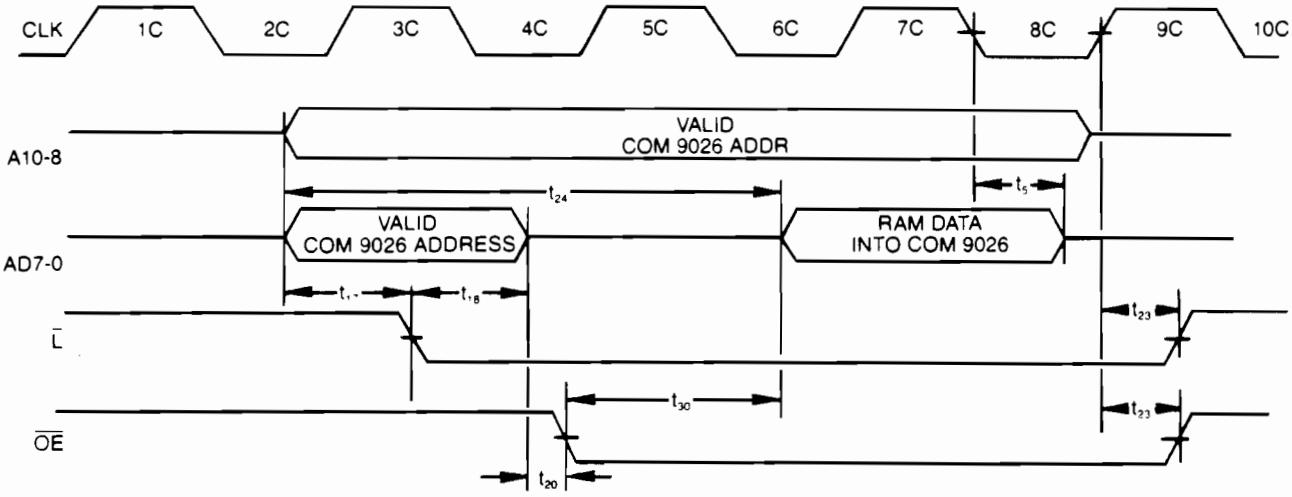


FIGURE 15—COM 9026 READ RAM AC TIMING

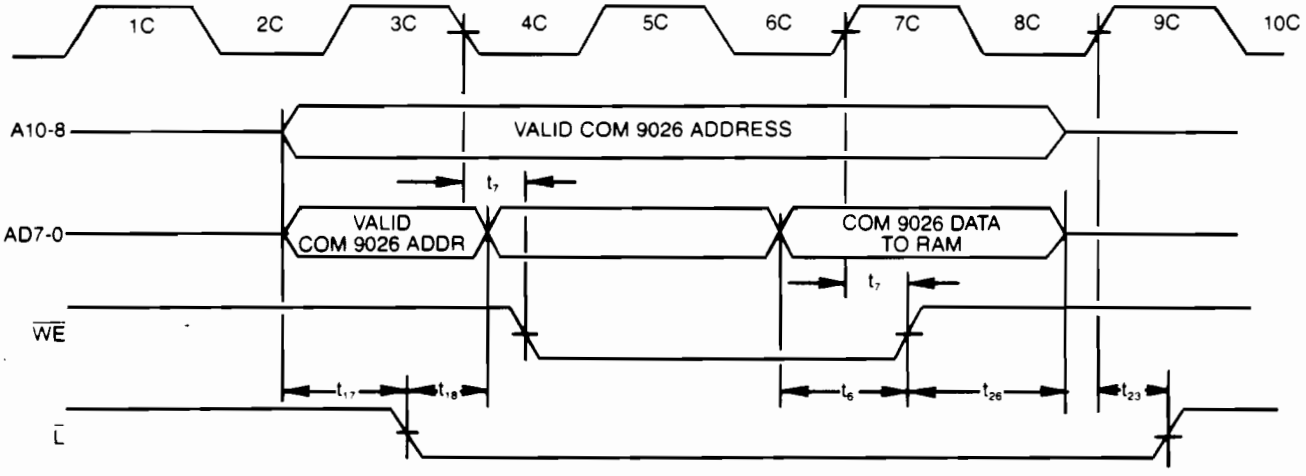


FIGURE 16—COM 9026 WRITE RAM AC TIMING

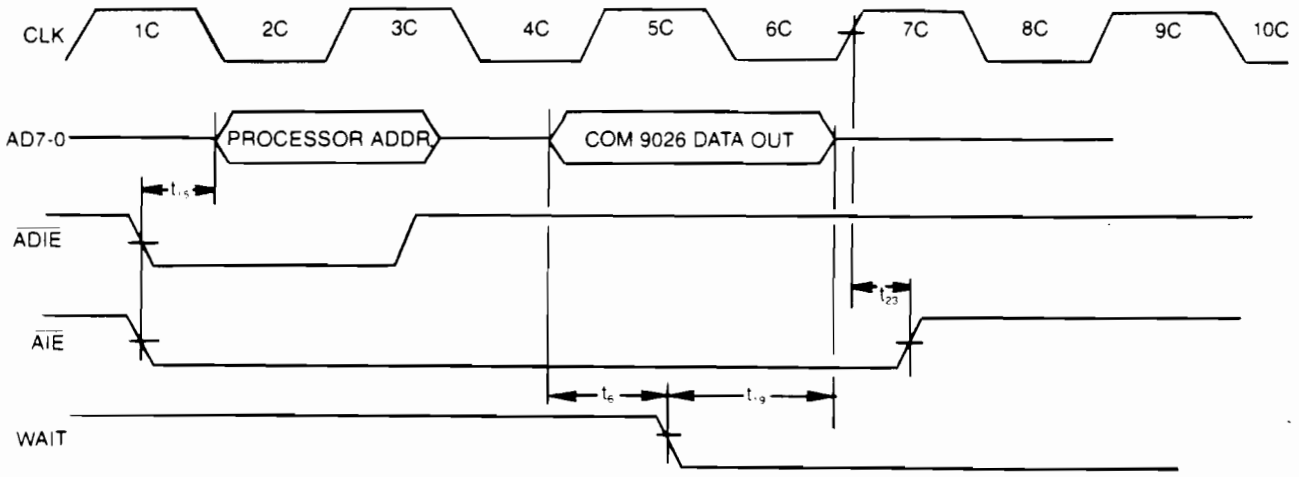


FIGURE 17—PROCESSOR READ COM 9026 AC TIMING

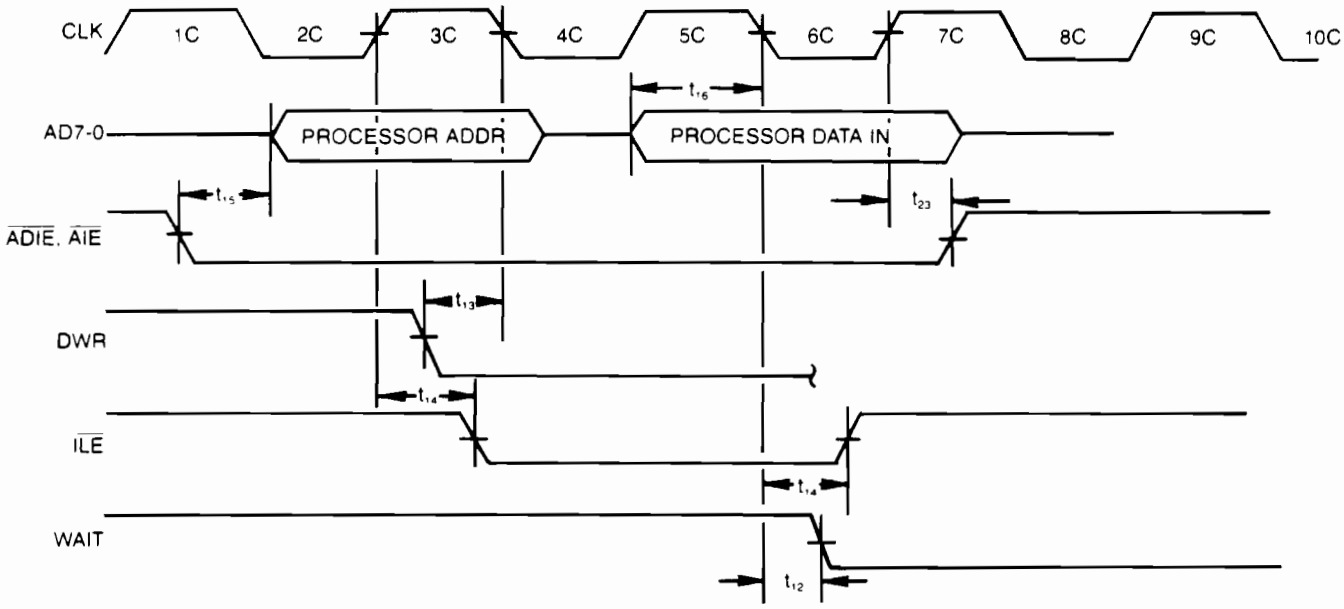


FIGURE 18—PROCESSOR WRITE COM 9026 AC TIMING

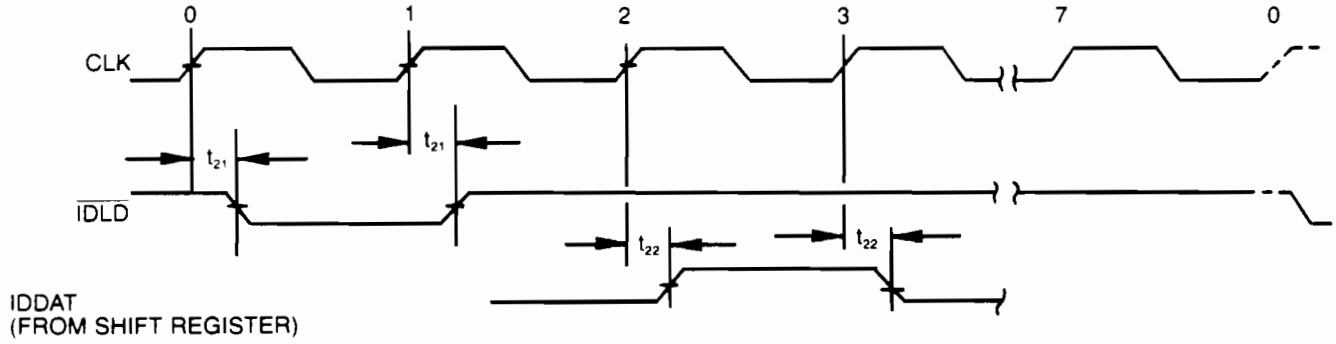


FIGURE 19—ID INPUT AC TIMING

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

TECHNICAL NOTE TN5-2

USING THE COM 9026 LOCAL AREA NETWORK CONTROLLER AND THE COM 9032 LOCAL AREA NETWORK TRANSCEIVER

The purpose of this technical note is to provide the information and schematics needed to implement the CLOCK GENERATOR and the CABLE TRANSCEIVER for the COM 9026. In addition, some discussion of the transmission media network topology and network performance is included.

CLOCK GENERATOR

Figures 1 and 2 illustrate the CLOCK GENERATOR and associated timing respectively. The purpose of this circuitry is to generate the CLK and CA signals for the COM 9026. A 20 MHz oscillator is used to allow proper control of the starting and stopping of the CA signal. The CLK signal is generated from a divide by 4 circuit using 2 74S112's.

The line protocol of the COM 9026 is designed to ensure that a negative transition always occurs 1 bit time before a particular byte of any transmission. A three bit field of 110, which proceeds every byte, provides the required negative transition. The "0" in this three bit field may be thought of as a start bit and the "11" may be thought of as two stop bits from the previous byte. When the COM 9026 is waiting for another byte (or the first byte) within a message, it will resynchronize the CA clock by temporarily halting the CA clock at the high level. It accomplishes this by lowering the $\overline{\text{DSYNC}}$ signal. When the RX line experiences a high to low transition (the "0" in the three bit field), the CA clock is restarted which in turn causes the $\overline{\text{DSYNC}}$ signal to be raised to the high level. The circuitry of figure 1 assumes an RX bit spacing of 400 nanoseconds which must be equal to twice the period of the CA clock. The circuitry of figure 1 is set up such that the next low to high transition of the CA clock occurs between 200 and 250 nanoseconds after the high to low transition on RX. This places the point at which the COM 9026 samples the RX input approximately midway into the bit. Every other low to high transition on CA thereafter will be used to sample the 8 bit data byte that follows. Once the byte is received, the $\overline{\text{DSYNC}}$ signal is again activated in preparation for the next high to low transition on the RX line indicating the start of the next data byte. The $\overline{\text{DSYNC}}$ output will return to its high (inactive) state after each CA synchronization is established. Figure 3 illustrates the relationship of the $\overline{\text{DSYNC}}$, CA and RX signals before, during, and after CA synchronization.

The technique used for synchronization is similar to that of standard asynchronous protocols where a sample point within an asynchronous signal is found and used for each byte transmitted. Traditionally, a 16X or 64X clock is used to provide the resolution needed to find the proper sample point for low frequency transmission. Because of the 2.5 M bit rate provided by the COM 9026, a 2X clock (the CA signal) is used in conjunction with an external 8X clock (20 MHz) to allow determination of a reliable sample point.

It should be noted that the $\overline{\text{DSYNC}}$ output can never become active low during a COM 9026 transmission. At the end of a transmission, the COM 9026 will wait about 6 microseconds. By this time the line should be quiet and the RX input will be sitting in a space (low) condition. At this time, the COM 9026 will wait for the RX input to become high (level sensitive not edge sensitive) which occurs during the alert burst of the next transmission. At this time, the COM 9026 starts reception by lowering the $\overline{\text{DSYNC}}$ signal.

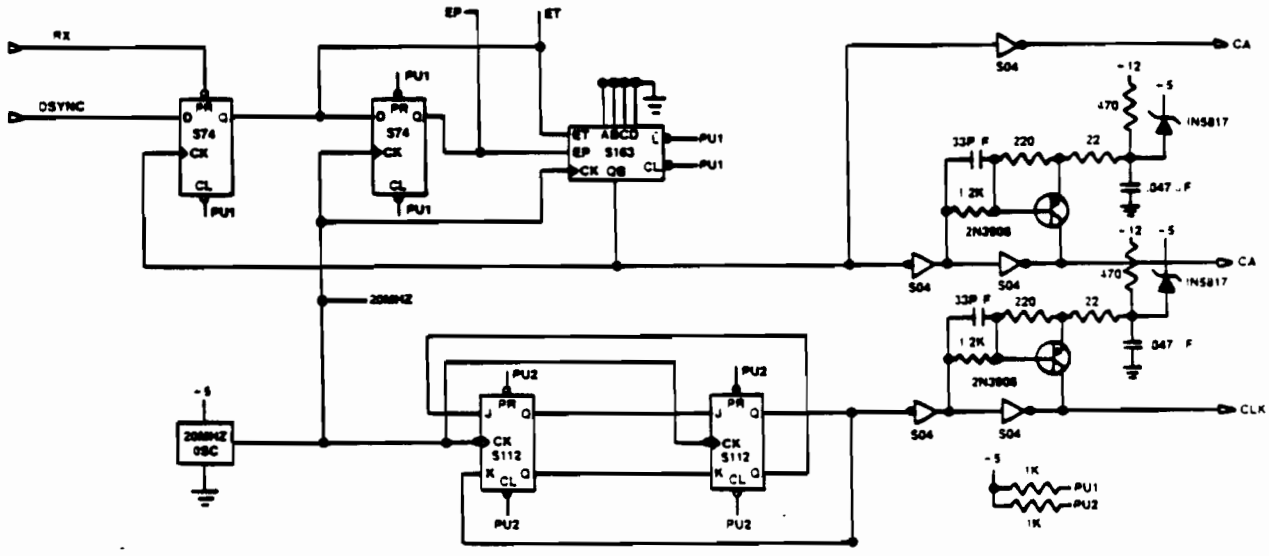


FIGURE 1: CLOCK GENERATION*

*Suggested circuit when using the COM9026 without the COM9032.

CABLE TRANSCEIVER

The circuitry of figure 1 and the COM 9026 assume the data appearing on the RX signal is NRZ with a high level indicating a logic "1" and a low level indicating a logic "0". The bit boundaries are spaced at 400 nanosecond intervals, establishing the 2.5 M bit data rate. The COM 9026, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds in duration to indicate a logic "1" and no pulse to indicate a logic "0". Figure 5 illustrates a typical data transmission.

The CABLE TRANSCEIVER's function is first to convert the 200 nanosecond $\overline{TX}$ pulses output by the COM 9026 to a format consistant with the transmission media and network topology and, second, to convert signals from the cable to the NRZ data required by the COM 9026's RX input. Starting with the $\overline{TX}$ and RX signals, many different cable transceiver implementations can result to allow for broadband or baseband networks using twisted pair, coax, or fiber optics as the transmission media. Figures 4 and 6 illustrate a typical CABLE TRANSCEIVER used to implement Datapoint's ARCNET* local area network. The ARCNET* implementation uses a baseband system with RG62 (93 ohm) coax.

Referring to figure 4, a 200 nanosecond negative pulse on $\overline{TX}$ is converted to two 100 nanosecond negative pulses shown as $\overline{PULSE\ 1}$ and $\overline{PULSE\ 2}$. These two signals are used to create a 200 nanosecond wide dipulse signal by being driven into opposite sides of RF transformer T1 and finally coupled onto the coax as shown in figure 6. Figure 7 shows the timing relationship between CA, $\overline{TX}$, $\overline{PULSE\ 1}$ and $\overline{PULSE\ 2}$. The waveform of the resultant dipulse is also shown in figure 7.

Referring to figure 6, a dipulse appearing on the coax is coupled to the receiver via RF transformer T1 and passed through a filter network matched to the 93 ohm characteristic impedance of the coax. The filter output feeds a 75108 comparator which produces a positive pulse on RCVD for each dipulse received from the coax. The RCVD signal feeds the circuitry shown in figure 4 which converts these pulses to NRZ data on the RX signal entering the COM 9026. Figure 8 illustrates the timing associated with this function.

The CABLE TRANSCEIVER shown in figures 4 and 6 has been designed to operate in a baseband cable system using a network topology where any 2 nodes are connected by a single path which is terminated at both ends with the cable's characteristic impedance. Figure 9 illustrates a typical free forming tree topology which is used in the ARCNET* implementation. By using central HUBs, each node connects through a length of cable to a port on a HUB with the cable terminated as previously described. No taps are used on the coax.

The COM 9032 local area network transceiver, housed in a 16 pin package, can replace all the logic shown in figures 1 and 4 and simplify the building of ARCNET* compatible networks by performing the following functions:

1- Generation of CA and CLK clocks for the COM 9026 with high voltage drive.
2- Creation of $\overline{PULSE\ 1}$ and $\overline{PULSE\ 2}$ waveforms during transmit.
3- Conversion of received data to NRZ format.

These functions are performed exactly as the TTL implementation shown in figures 1 and 4. Figure 10 illustrates the COM 9032 used with the COM 9026 to implement an ARCNET* compatible cable transceiver.

*ARCNET is a registered trademark of the Datapoint Corporation

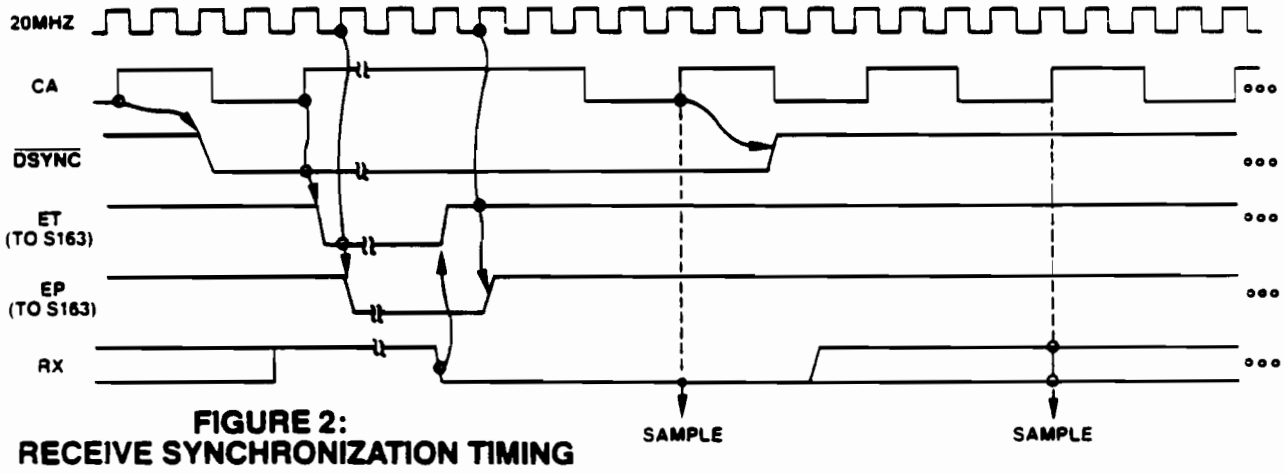


FIGURE 2: RECEIVE SYNCHRONIZATION TIMING

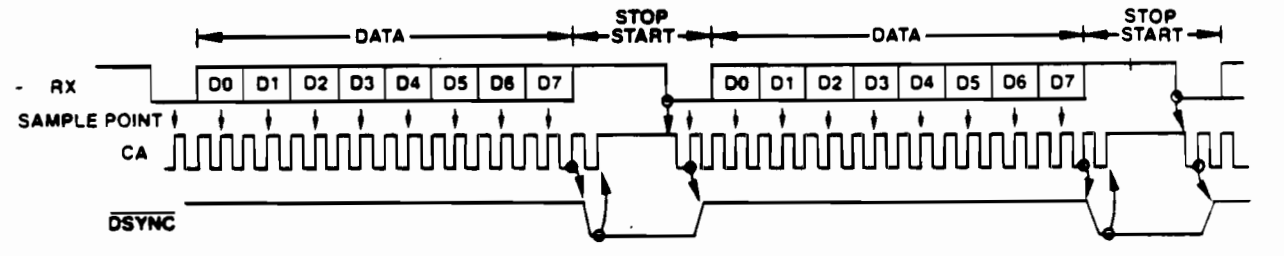


FIGURE 3: BYTE TO BYTE RECEIVE SYNCHRONIZATION

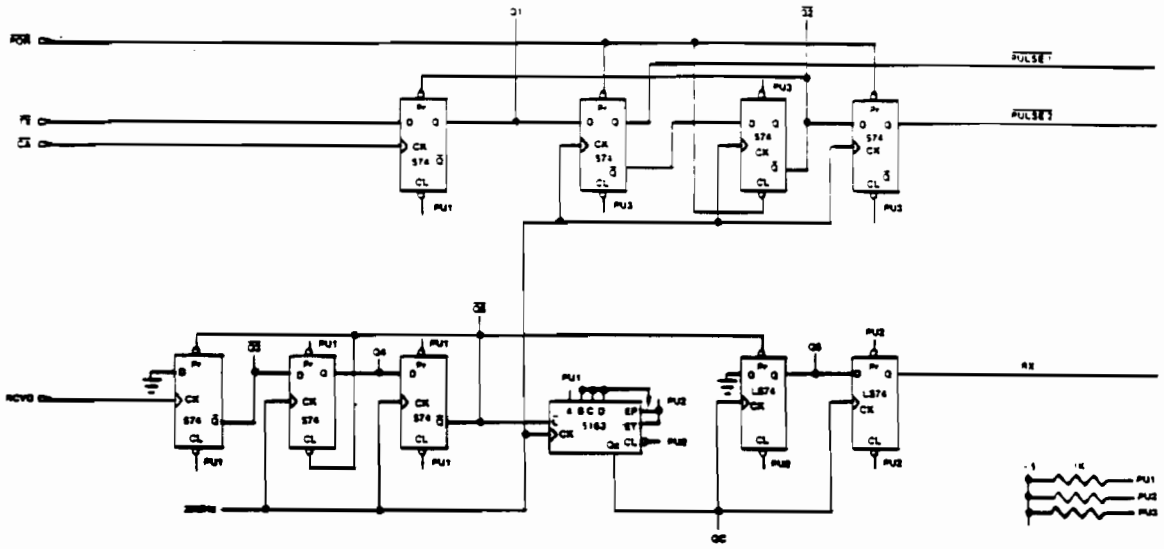


FIGURE 4: TRANSMIT AND RECEIVE LOGIC*

*Suggested circuit when using the COM9026 without the COM9032.

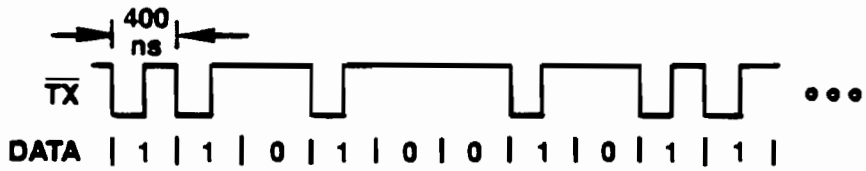


FIGURE 5: TYPICAL $\overline{TX}$ WAVEFORM

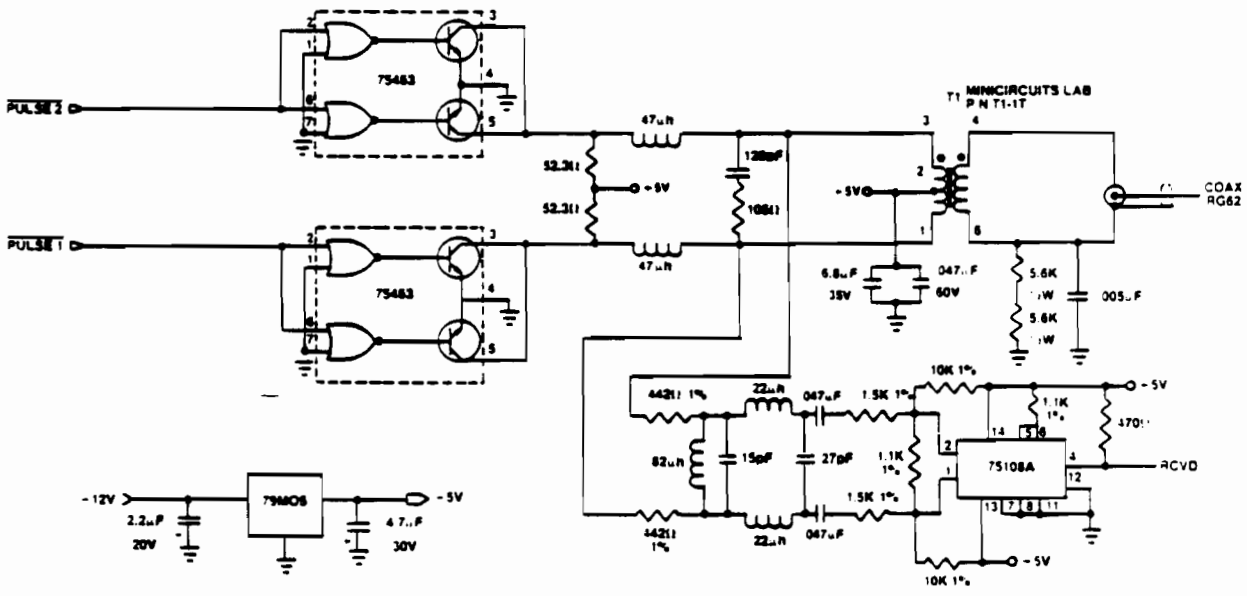


FIGURE 6: ARCNET* CABLE TRANSCEIVER

*ARCNET is a registered trademark of the Datapoint Corporation

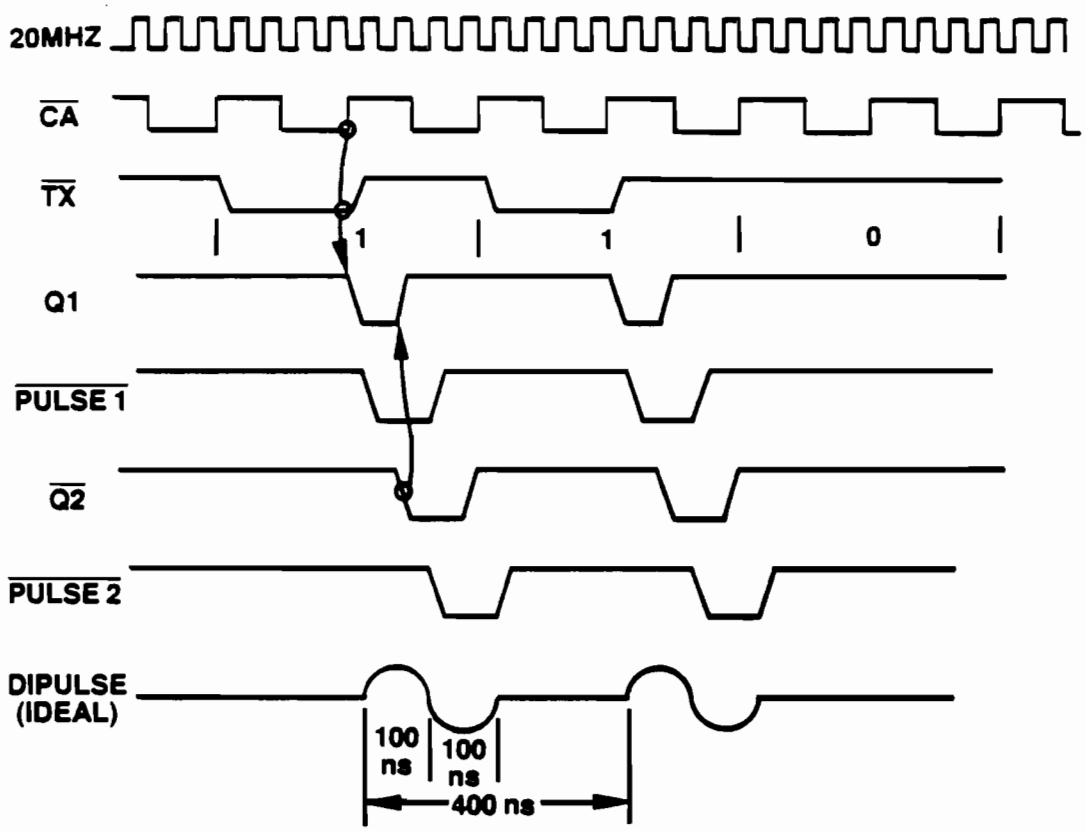


FIGURE 7: DIPULSE GENERATION

FIGURE 8: RX WAVEFORM GENERATION

HUB ELECTRONICS

Figures 11a and 11b illustrate a typical implementation of an active HUB. The HUB may be thought of as an amplifier and a number of ideal taps mounted in the same box. Each tap is ideal in that it causes no insertion loss, no tap loss and provides total suppression of reflections. Each of the ports on the HUB may be connected to a network node, to another HUB, to an unterminated length of coax, or to nothing at all. The reflections caused by connecting an unterminated length of coax is taken into account in the HUB implementation and will not have any negative effects on network operation.

When no activity appears on the HUB ports, the HUB enters the idle state and all receivers are enabled. This state corresponds to a clear condition within the octal register which provides disable signals to the transmitters of all ports through the interface modules. As soon as any port senses activity (port n), one of 8 74S74's is clocked low causing the output of AND 1 to go low. This in turn brings the signal SET to a high which causes the octal register to be clocked through AND 2. The clocking of the octal register causes one output to remain low (the one corresponding to the port which sensed activity designated as port n) and the other seven outputs to go high. This allows port n to transmit (repeat) its signal to all other ports. For each pulse sensed, the delay module will generate $\overline{\text{PULSE 1}}$ and $\overline{\text{PULSE 2}}$ which is used by all other ports to generate the dipulse as shown in figure 7. The HUB remains in this active state until the transmission it is repeating is finished. At this time it returns to the idle state.

The determination of when a transmission is finished is based on time. There are never more than nine consecutive spacing elements in a transmission (the start element and eight zeros). Therefore, a dipulse is received at least once every ten unit intervals (4 microseconds). The COM 9026 has a turnaround time somewhat greater than 12 microseconds so there will be at least a 12 microsecond interval of no activity between the end of the last data element of one transmission and the start of the alert burst of the next transmission. Were it not for the potential reflection problem caused by an unterminated or unconnected length of coax, the HUB could drop back into the idle state when the receiver has not heard anything for some period of time between 4 and 12 microseconds.

In order to provide protection against reflections, the HUB should not fall back into the idle state until any and all reflections cease. For individual runs of coax not greater than 2000 feet (RG62 coax), a reflection from a shorted or unterminated cable will return in less than 4.9 microseconds. Changing the 4 microsecond limit to 4.9 microseconds will allow the HUB and the network to be unaffected by reflections. For the duration of the packet, retriggerable one shot OS1 will never fire. The 5.5 microsecond duration of OS1 will determine when a packet transmission has concluded by sensing a lack of activity for greater than 4.9 microseconds. When OS1 fires, OS2 produces a 150 nanosecond pulse which resets the octal register, resets the signal SET and clears all 8 74S74's. This corresponds to the idle state of the HUB and the process repeats when the next packet is received.

It is possible to implement a passive HUB as shown in figure 12. This arrangement allows for a maximum of 4 ports. For proper operation, each port must be terminated in 93 ohms either by connecting it to an active node or attaching a 93 ohm BNC terminator to the unconnected port. When the ports are terminated properly, each port will have an input impedance of 93 ohms. Due to the considerable loss experienced in this arrangement, it is recommended that no more than 4 nodes be connected in this manner.

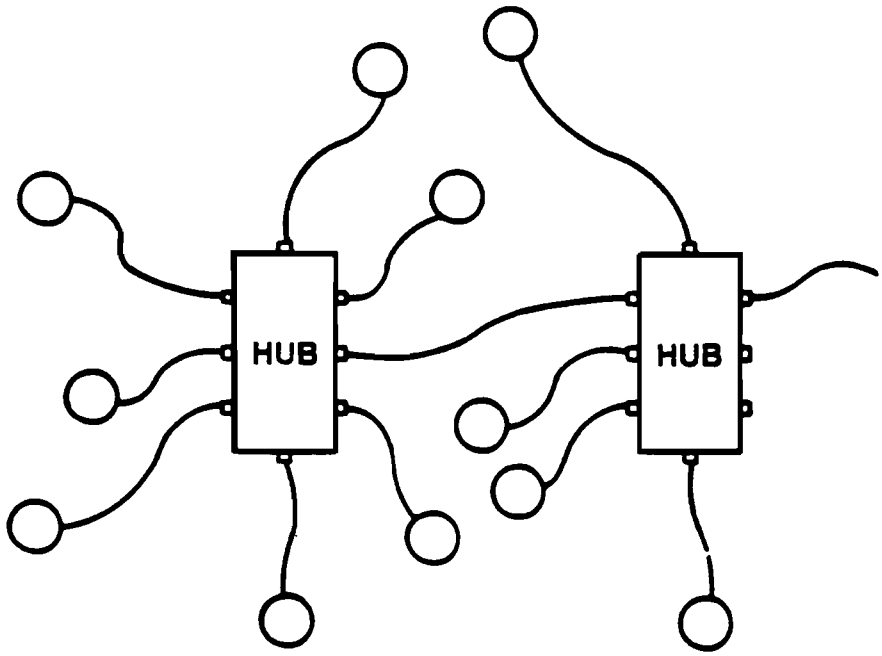


FIGURE 9: TYPICAL NETWORK TOPOLOGY

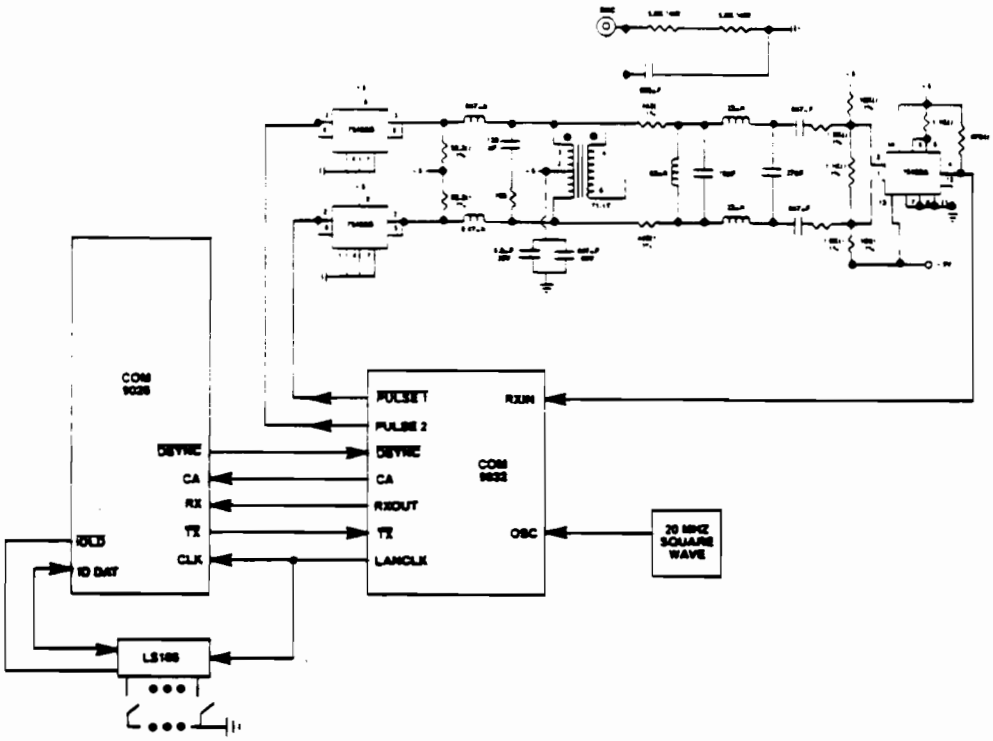
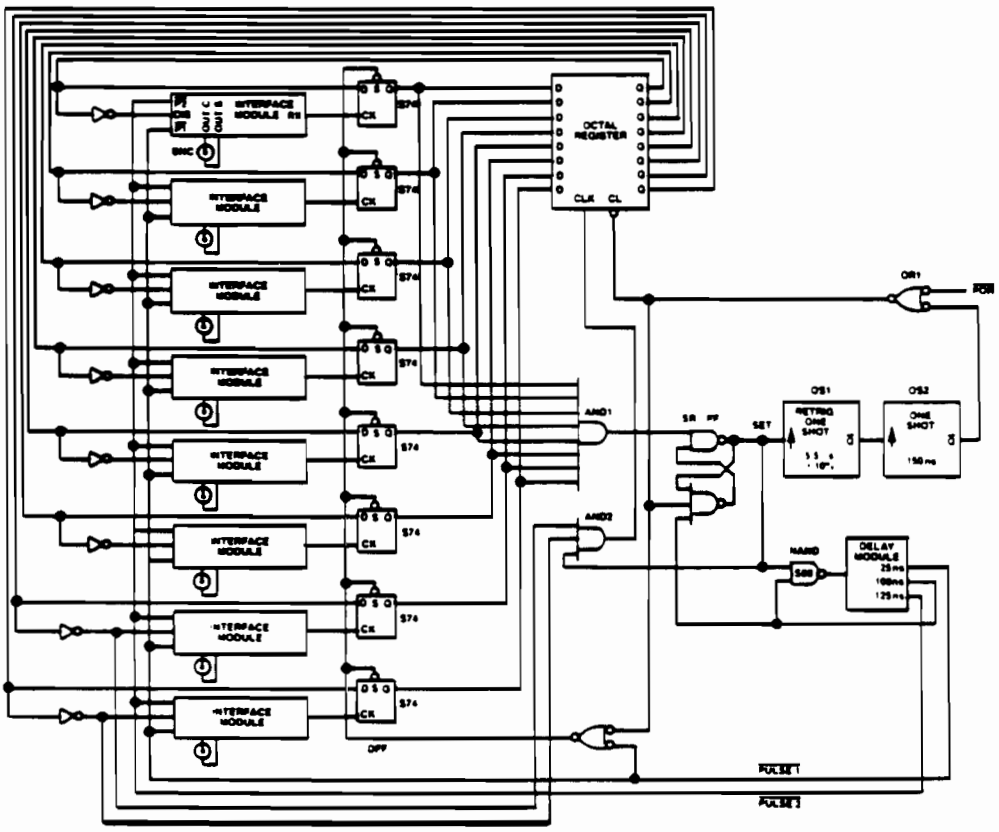
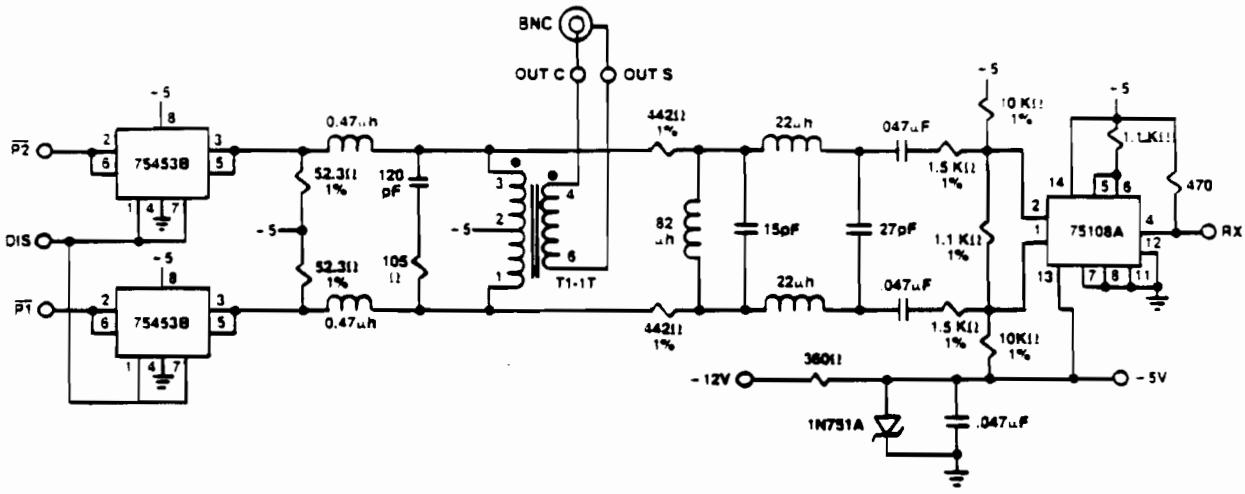


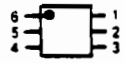
FIGURE 10: ARCNET* COMPATIBLE CABLE TRANSCEIVER USING THE COM 9032



*ARCNET is a registered trademark of the Datapoint Corporation



T1-1T TOP VIEW
(MINICIRCUITS LAB)



NOTE: T1-1T PIN NOS. DIFFER FROM NORMAL IC.

FIGURE 11B: TYPICAL ACTIVE HUB ELECTRONICS (INTERFACE MODULE)

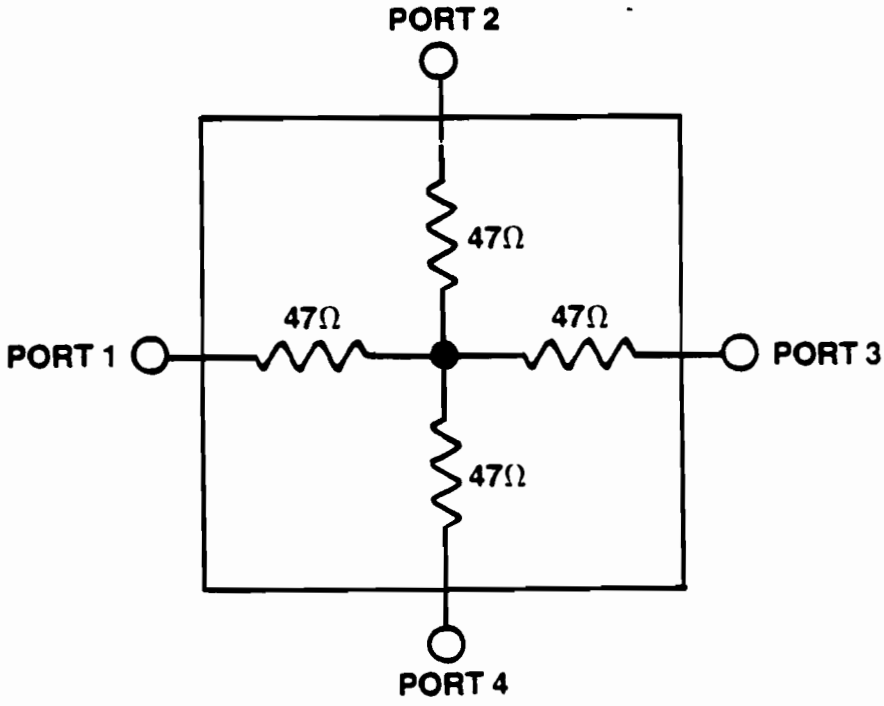


FIGURE 12: 4 PORT PASSIVE HUB

Packet Transmission

Transmission of a message begins with the processor selecting a page in the RAM buffer and writing the packet. Figure 13 illustrates the RAM buffer format for a message of length 120 (78 HEX) from ID #4C HEX to ID #B2 HEX. Note that address 02 of the selected page contains the 2's complement of the number of data bytes in the message. Figure 14 illustrates the RAM buffer format for a message of length 300 (12C HEX; long packet) from ID #2F to ID #D8. Note that address 02 must contain all zeros with address 03 equal to the 2's complement of the number of data bytes in the message. The 2's complement for long packets is calculated with respect to 512 but only 8 bits are used in RAM buffer address 03. The COM 9026 will keep track of the 9th bit internally. The RAM buffer is arranged such that the last data byte will always reside in address 255 (FF HEX) for short packets and address 511 (1FF HEX) for long packets. Broadcast messages will be transmitted if address 01 is set to 00.

Once the buffer is loaded, the processor must wait for the TA status bit to become a logic one. The TA bit informs the processor that a previous transmit command has concluded and another transmit command can be issued. Each time the message is loaded and a transmit command issued, it will take a variable amount of time before the message is transmitted depending on the traffic on the network and the location of the token at the time the transmit command was issued. Typically, the conclusion of the transmit command, which is flagged when TA becomes a logic one, generates an interrupt. While waiting for the interrupt to occur, the processor can load another page in the RAM buffer with the next message to be sent in anticipation of the transmitter becoming available (TA becomes a logic one). In this way, double buffering is accomplished by loading a second message while the first message is being transmitted. The interrupt will then allow the software to time the repeated issuing of transmit commands.

Before a message is transmitted, the destination node is asked if it is able to receive the message via a FREE BUFFER ENQUIRY transmission. This is done automatically by the COM 9026 with no software intervention. If the destination node is not servicing its COM 9026, for whatever reason, the receiver at the destination node will be inhibited (RI set to a logic one) and the source node will never be able to deliver the packet and set the TA bit to a logic one. Because of this, there should be a software timeout on the TA bit. When the timer times out, the processor should disable the transmitter which forces the COM 9026 to abandon the transmission and causes the TA bit to set to a logic one when the node next receives the token. If the source node attempts to transmit a packet to a nonexistent node, the packet will never be delivered but the TA bit will always be set to a logic one. In this situation, the TMA bit will never get set.

If the disable transmitter command does not cause the TA bit to be set in the time it takes the token to make a round trip through the network, it will indicate one of three situations:

1-The node is disconnected from the network.
2-There are no other active nodes on the network.
3-The external receive circuitry has failed.

These situations can be determined by using another software timeout which is greater than the worst case time for a round trip token pass which occurs when all nodes transmit a maximum length message.

It should be noted that each node, upon packet transmission, ignores the value of the SID in the buffer and instead inserts the ID number as specified by the external switches.

Packet Reception

To enable the receiver for packet reception, the processor selects a page in the buffer to use and waits for the RI status bit to become a logic one. The RI bit informs the processor that a previous RECEIVE command has concluded and another RECEIVE command can be issued. Each time a receive command is issued, the reception can take a variable length of time since there is no way of telling when another node will decide to transmit a message directed at this node. The RECEIVE command will reserve a particular page of memory in the RAM buffer for reception. Only the successful reception of a packet, or the issuing of a DISABLE RECEIVE command will set the RI bit to a logic one, thus freeing up the page in the RAM buffer for processor accesses.

ADDRESS	DATA
00	4C
01	B2
02	88(= 100-78)
.	.
.	.
.	.
88	DATA BYTE 1
89	DATA BYTE 2
8A	DATA BYTE 3
.	.
.	.
.	.
FF	DATA BYTE 120

FIGURE 13: TYPICAL SHORT PACKET BUFFER FOR TRANSMIT

ADDRESS	DATA
00	2F
01	D8
02	00
03	D4(= 200-12C)
.	.
.	.
.	.
D4	DATA BYTE 1
D5	DATA BYTE 2
D6	DATA BYTE 3
.	.
.	.
.	.
1FF	DATA BYTE 300

FIGURE 14: TYPICAL LONG PACKET BUFFER FOR TRANSMIT

Typically, the conclusion of a RECEIVE command, which is flagged by the RI bit being set to a logic one, will generate an interrupt and allow the processor to read or operate on the message as required. Figure 15 illustrates the contents of a page in the RAM buffer after a packet is received for a source ID # of F3 and a destination ID # of 91 with a packet length of 201 bytes (C9 HEX). Figure 16 illustrates the contents on the RAM buffer after a packet is received from a source ID # of C3 and a destination ID # of 1F with a packet length of 490 bytes (1EA HEX). The COM 9026 will deposit packets in the RAM buffer in a format identical to the transmit format allowing for a message to be received and then retransmitted without rearranging any bytes in the RAM buffer.

COM 9026 Interrupts

When using the interrupt structure of the COM 9026 to time the issuing of the transmit and receive commands, certain procedures should be followed. The INT output of the COM 9026 is generated in a variety of ways. For the transmitter, the INT output is generated by the logic function TA anded with bit zero in the interrupt mask register. Assuming the mask register bit is set to a logic one, allowing transmitter interrupts to occur, when the TA bit gets set to a logic one, the interrupt is simultaneously generated. In order to clear the interrupt and prevent repeated servicing of the same interrupt, either another transmit command should be loaded (if there is another message ready to be transmitted) which will reset the TA bit to a logic zero, or bit zero of the interrupt mask register should be reset to a logic zero.

During reception, the INT output is generated by the logic function RI anded with bit 7 of the interrupt mask register. Assuming the mask register bit 7 is set to a logic one, allowing receive interrupts to occur, when the RI bit gets set to a logic one, an interrupt is simultaneously generated. As for the transmitter, the interrupt should be cleared during the interrupt service routine. The clearing of the interrupt is accomplished by either issuing another receive command (if a page in the RAM buffer has been freed up to accept a new data packet) or by resetting bit 7 of the interrupt mask register to a logic zero.

Network Performance

The most important parameter used to measure performance in a local area network is the amount of time a node has to wait before being able to send a message. This parameter actually denotes the number of messages per second leaving each node. In the token passing scheme used by the COM 9026, this wait time is bounded by the time it takes the token to make a round trip through each node on the network. This time is a function of the number of nodes on the network, the traffic activity, and the number of bytes transmitted in each message. There are also some delay times that are intrinsic to the COM 9026 contributing to this wait time.

The COM 9026 will perform a simple token pass (it receives the token, has nothing to transmit and passes the token to the Next ID) in approximately 28 microseconds. Therefore, the best time for a round trip token pass to each node can be expressed as follows:

$$Tb = 28N \text{ microseconds}$$

where N equals the number of nodes on the network. When a particular node receives the token and has a message to transmit, the COM 9026 introduces an additional time of 113 microseconds plus 4.4 microseconds for each byte transmitted in the message. Therefore, the worst case time for a round trip token pass, which exists when each node on the network has a message to transmit, can be expressed as follows:

$$Tw = Tb + (113 - 4.4B)N \text{ microseconds}$$

where B equals the average number of bytes sent per message. Combining terms, the wait time, Twait, is bounded by the following equation:

$$28N < Twait < (141 - 4.4B)N \text{ microseconds}$$

In a typical network consisting of 10 nodes with an average message length of 100 bytes, Twait will fall between 280 microseconds (no messages sent) and 5.81 milliseconds (when all 10 nodes send 100 byte messages). If only a single node is sending messages, it can send one every 833 microseconds; a rate of 1200 messages per second or 120,000 bytes per second. If all 10 nodes send 100 byte messages, each node will be able to send a message every 5.81 milliseconds; a rate of 172 messages per second or 17,200 bytes per second.

In actual practice, Datapoint Corporation has installed many ARCNET systems with as many as 200 nodes active at any given time. A typical network supports two totally independent operating systems and a wide variety of uses including program loading, word processing, print spooling, program development, electronic mail, etc. The traffic load on this type network rarely falls below 400 messages

ADDRESS	DATA
00	F3
01	91
02	37(= 100-C9)
:	:
37	DATA BYTE 1
38	DATA BYTE 2
39	DATA BYTE 3
:	:
FF	DATA BYTE 201

FIGURE 15: TYPICAL SHORT PACKET BUFFER AFTER RECEPTION

ADDRESS	DATA
00	C3
01	1F
02	00
03	16(= 200-1EA)
:	:
16	DATA BYTE 1
17	DATA BYTE 2
18	DATA BYTE 3
:	:
1FF	DATA BYTE 490

FIGURE 16: TYPICAL LONG PACKET BUFFER AFTER RECEPTION

per second, yet less than 2% of the nodes send a message on any single token trip. The time required for a token trip, therefore, stays very close to the no traffic value with peaks of three times the no traffic value being extremely rare.

The COM 9026 has some interesting features that allow one to monitor the dynamic performance of the network from any node. During any message transmission, each node will receive the source ID (SID) and destination ID (DID) and store the SID into RAM buffer location 02 of the current page enabled for receive. If the message is not directed at the particular node, the message itself is not deposited into the RAM buffer. Every node, therefore, will store at least the source of every message sent on the network making it possible to monitor the traffic activity.

In addition, continual loading of a TRANSMIT command followed immediately by a DISABLE TRANSMIT command makes it possible to measure the time for one complete token pass. Once the DISABLE TRANSMIT command is loaded, the command will not actually end until the node next receives the token. In this case, the TA bit in the status register is used to inform the host processor that the token has been passed through the node since only receipt of the token will allow the DISABLE TRANSMIT command to be completed. By measuring the time between successive settings of the TA status bit, an accurate measure of the time for every round trip token pass can be determined.

A NETWORK RECONFIGURATION occurs whenever a new network node is first activated onto the system. In the normal course of events, nodes are always being activated, and the system adjusts this by initiating a NETWORK RECONFIGURATION. The time to complete a NETWORK RECONFIGURATION and return to a normal operating environment is a function of the propagation delay between nodes, the number of nodes on the network, and the highest ID number on the network. Figure 17 is a graph illustrating the reconfiguration time as a function of the number of nodes on the network and the highest ID number and shows a range of 21 to 61 milliseconds. The reconfiguration time shown assumes no cable propagation delay. The reconfiguration time has no long lasting effect on the system performance and will only increase the time of a single token pass by the actual time of reconfiguration.

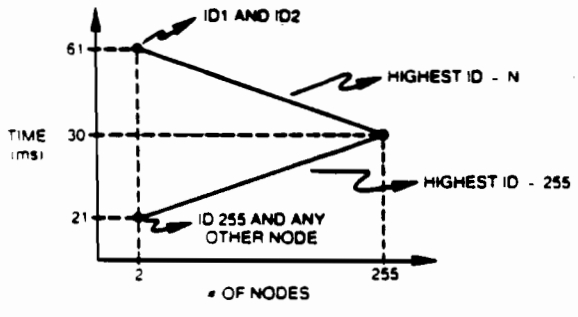


FIGURE 17:
NETWORK RECONFIGURATION TIME

Similarly, when a node is deactivated, the node that usually passes the token will have to continually try to pass the token to the next highest ID. The time it takes for a node to pass the token and find the next active node is a function of the difference in ID numbers of the deactivated node and the next highest active node. For example, if node #3 passes to node #10 and node #10 passes to node #20, and if node #10 is deactivated, then node #3 will issue an INVITATION TO TRANSMIT to nodes 10, 11, 12,...etc. and finally node 20 where it will detect line activity and complete the token pass. In this example, node #3 will issue eleven INVITATION's TO TRANSMIT, all but the last one taking 93.6 microseconds (see appendix 1; TOKEN PASS with no response), before finally finding activity at node #20. In this example, the extra time associated with this system adjustment will be 10 times 93.6 microseconds plus the response time of the active node which must be less than 74 microseconds assuming a one way cable propagation delay of 31 microseconds. Just as with the NETWORK RECONFIGURATION, this adjustment has no long lasting effect on the system performance and will only increase the time of a single token pass by an amount equal to the time taken to find the next active node on the network.

For a more detailed discussion of the critical performance parameters, refer to appendix 1.

Extended Length Message Operation

The COM 9026 can transmit and receive short packets (maximum length of 253 bytes) or long packets (maximum length of 508 bytes). When only short packets are used, it is possible to use either a 1K or 2K RAM buffer. When both long and short packets are used, a 2K RAM buffer must be used.

Use of the extended length message feature is controlled via the DEFINE CONFIGURATION command. This command allows the user to set the long packet enable flag. When this flag is set and the contents of RAM buffer address 02 is zero, the packet is treated as a long packet with RAM buffer address 03 pointing to the address containing the first byte in the message. In this case, the last byte in the message resides in RAM buffer address 511. When the long packet enable flag is set, both long and short packets can be handled. However, when the long packet enable flag is reset, only short packets can be handled.

Whatever the packet length, the COUNT byte will always point to an address situated in the first 256 bytes of the page selected. Because of this, message lengths of 254 through 256 bytes must be padded out to a length of at least 257 bytes in order to be handled.

Nodes equipped and configured for extended length messages can coexist in the same system as nodes not configured for extended length messages. The DEFINE CONFIGURATION command merely informs the COM 9026 of the existence of an external 2K buffer and thus need only be issued at initialization time. Operation with standard length messages (less than 254 bytes) proceeds in the normal fashion.

If an extended length message is sent to a node that does not have its long packet enable flag set, the receiver will ignore it. The transmitting COM 9026 will set its TA bit but not the TMA bit. If an attempt is made to have a node transmit an extended length message when the node does not have its long packet enable flag set, the packet will not be sent and the TA bit will stay off until a DISABLE TRANSMITTER command is issued. To the host processor, this situation will appear exactly as if a transmission were attempted to a node that has its receiver inhibited.

APPENDIX 1: DETAILED TIMING INFORMATION

The following information is provided for the benefit of users wishing to perform their own performance analysis. The equations shown in the section entitled NETWORK PERFORMANCE have assumed no cable propagation delay. The information that follows will accurately include all cable delays.

The lengths of the five types of COM 9026 transmissions are shown below:

INVITATIONS TO TRANSMIT (ITT)

ALERT BURST	= 2.4 µs (6 bits)
EOT, DID, DID	= 13.2 µs (33 bits)
	15.6 µs

FREE BUFFER ENQUIRIES (FBE)

ALERT BURST	= 2.4 µs (6 bits)
ENQ, DID, DID	= 13.2 µs (33 bits)
	15.6 µs

PACKETS (PAC)

ALERT BURST	= 2.4 µs (6 bits)
SOH, SID, DID, DID, COUNT	= 22.0 µs (55 bits)
B CHARACTERS	= 4.48 µs (55B bits)
CRC, CRC	= 8.8 µs (22 bits)
	33.2 µs + 4.48 µs

ACKNOWLEDGEMENTS (ACK)

ALERT BURST	= 2.4 µs (6 bits)
ACK	= 4.4 µs (11 bits)
	6.8 µs

NEGATIVE ACKNOWLEDGEMENTS (NAK)

ALERT BURST	= 2.4 µs (6 bits)
NAK	= 4.4 µs (11 bits)
	6.8 µs

In addition, there are certain delay constants and cable propagation times required for analysis as described below:

CHIP TURNAROUND TIME (Tta) = 12.6 µs

This time is defined as the time from the end of any received transmission until the start of a response.

TOKEN PROPAGATION DELAY (Tpt)

This time is defined as the CABLE propagation time between the node holding the token and the node receiving the token.

MESSAGE PROPAGATION TIME (Tpm)

This time is defined as the CABLE propagation time between the node holding the token and the node receiving a message.

BROADCAST DELAY TIME (Tbd) = 15.6 µs

This time is defined as the time from the end of a transmitted broadcast packet until the start of a token pass.

RESPONSE TIMEOUT (Trp)

This time is the maximum amount of a time a COM 9026 will wait for a response which should be greater than or equal to twice the maximum cable propagation delay (the delay between the two furthest nodes) plus the CHIP TURNAROUND TIME as defined above. This value is programmable using the ET1 and ET2 inputs.

RECOVERY TIME (Trc) = 3.4 µs

This time is the amount from the end of the RESPONSE TIMEOUT until the start of a token pass.

Given the above numbers, it is possible to calculate the time a token will "dwell" at any node. A number of cases are detailed below. In each case, the time calculated is the time from the start of one token pass to the start of the next token pass. For all cases a Trp of 74.6 µs is assumed.

SIMPLE TOKEN PASS (no message sent)

ITT	15.6 µs
Tta	12.6 µs + Tpt
	28.2 µs + Tpt

TOKEN PASS AND MESSAGE

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Tta	12.6 µs + Tpm
ACK	6.8 µs
Tta	12.6 µs + Tpm
PAC	33.2 µs + 4.48 µs
Tta	12.6 µs + Tpm
ACK	6.8 µs
Tta	12.6 µs + Tpm
	141.0 µs + 4.48 µs + Tpt + 4Tpm

TOKEN PASS AND MESSAGE (receiver inhibited)

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Tta	12.6 µs + Tpm
NAK	6.8 µs
Tta	12.6 µs + Tpm
	75.8 µs + Tpt + 2Tpm

TOKEN PASS AND MESSAGE (broadcast)

ITT	15.6 µs
Tta	12.6 µs + Tpt
PAC	33.2 µs + 4.48 µs
Tbd	15.6 µs
	77.0 µs + 4.48 µs + Ttp

TOKEN PASS AND MESSAGE (ACK gets lost)

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Tta	12.6 µs + Tpm
ACK	6.8 µs
Tta	12.6 µs + Tpm
PAC	33.2 µs + 4.4N µs
Trp	74.6 µs
Trc	3.4 µs
	187.0 µs + 4.48 µs + Tpt + 2Tpm

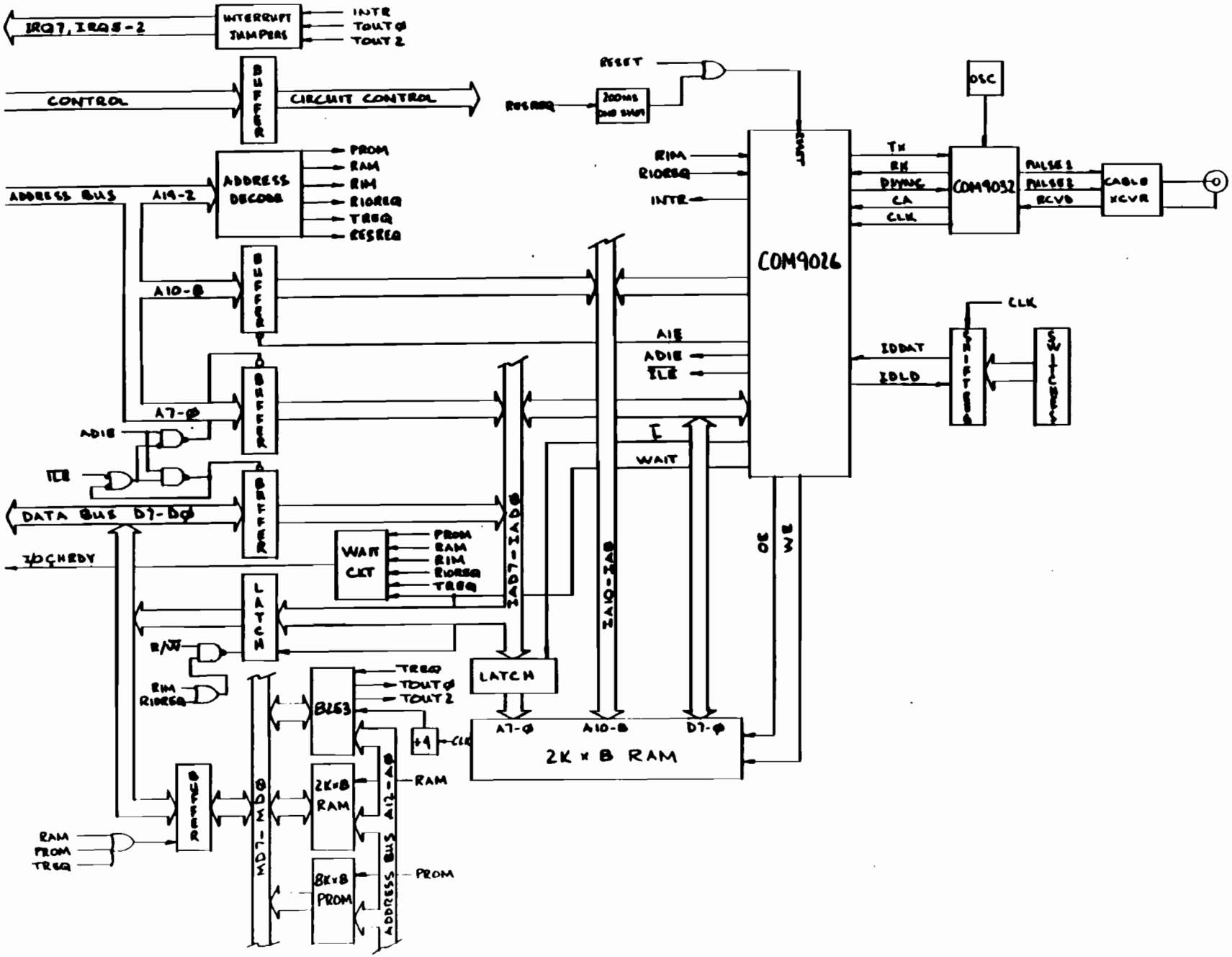
TOKEN PASS AND MESSAGE (destination node does not exist)

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Trp	74.8 µs
Trc	3.4 µs
	121.8 µs + Tpt

TOKEN PASS (no response)

ITT	15.6 µs
Trp	74.6 µs
Trc	3.4 µs
	93.6 µs

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, NY 11788 (516) 273-3100



ARCNET-PC BLOCK DIAGRAM